Low Power HART Modem

Data Sheet

AD5700/AD5700-1

FEATURES

- HART-compliant fully integrated FSK modem
- 1200 Hz and 2200 Hz sinusoidal shift frequencies
- 115 µA maximum supply current in receive mode
- Suitable for intrinsically safe applications
- Integrated receive band-pass filter
  - Minimal external components required
- Clocking optimized for various system configurations
  - Ultralow power crystal oscillator (60 µA maximum)
  - External CMOS clock source
  - Precision internal oscillator (AD5700-1 only)
- Buffered HART output—extra drive capability
- 8 kV HBM ESD rating
- 2 V to 5.5 V power supply
- 1.71 V to 5.5 V interface
- –40°C to +125°C operation
- 4 mm × 4 mm LFCSP package
- HART physical layer compliant
- UART interface

APPLICATIONS

- Field transmitters
- HART multiplexers
- PLC and DCS analog I/O modules
- HART network connectivity

GENERAL DESCRIPTION

The AD5700/AD5700-1 are single-chip solutions, designed and specified to operate as a HART® FSK half-duplex modem, complying with the HART physical layer requirements. The AD5700/AD5700-1 integrate all of the necessary filtering, signal detection, modulating, demodulating and signal generation functions, thus requiring few external components. The 0.5% precision internal oscillator on the AD5700-1 greatly reduces the board space requirements, making it ideal for line-powered applications in both master and slave configurations. The maximum supply current consumption is 115 µA, making the AD5700/AD5700-1 an optimal choice for low power loop-powered applications. Transmit waveforms are phase continuous 1200 Hz and 2200 Hz sinusoids. The AD5700/AD5700-1 contain accurate carrier detect circuitry and use a standard UART interface.

Table 1. Related Products

Part No.	Description
AD5755-1	Quad-channel, 16-bit, serial input, 4 mA to 20 mA and voltage output DAC, dynamic power control, HART connectivity
AD5421	16-bit, serial input, loop powered, 4 mA to 20 mA DAC
AD5410/ AD5420	Single-channel, 12-bit/16-bit, serial input, 4 mA to 20 mA current source DACs
AD5412/ AD5422	Single-channel, 12-bit/16-bit, serial input, current source and voltage output DACs

FUNCTIONAL BLOCK DIAGRAM

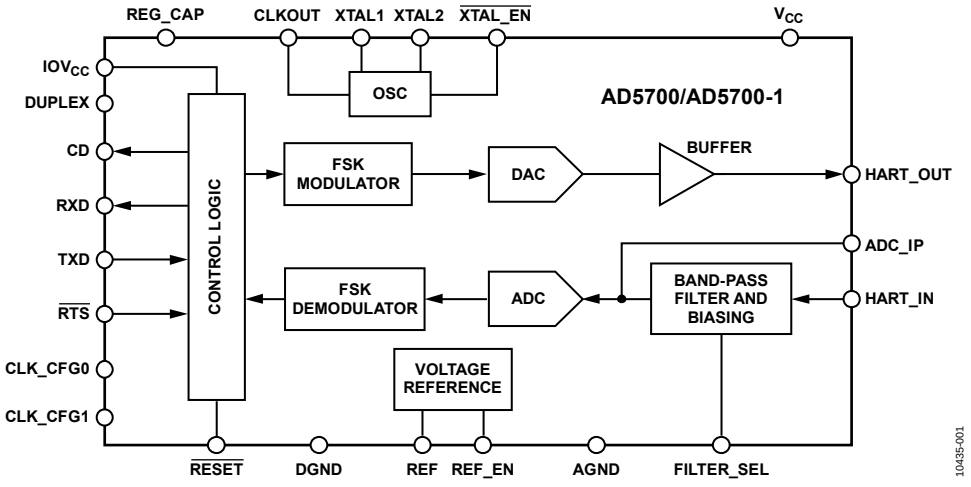

Figure 1.

HART® COMMUNICATION PROTOCOL

Rev. A

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REVISION HISTORY

4/12—Rev. 0 to Rev. A

Change to Transmit Impedance Parameter, $\overline{\text{RTS}}$ Low, Table 2 .. 4
Changes to Figure 3, Figure 4, Figure 5, and Figure 7 ... 9
Changes to Figure 10 and Figure 11 ... 10
Changed AD5755 to AD5755-1 Throughout ... 17
Change to Figure 27 ... 18

2/12—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 2 V to 5.5 V, IOV_{CC} = 1.71 V to 5.5 V, AGND = DGND, CLKOUT disabled, HART_OUT with 5 nF load, internal and external receive filter, internal reference, all specifications are from −40°C to +125°C and relate to both A and B models, unless otherwise noted.

Table 2.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS[2]					
V_{CC}	2		5.5	V	
IOV_{CC}	1.71		5.5	V	
V_{CC} and IOV_{CC} Current Consumption					
Demodulator		86	115	µA	B model, external clock, −40°C to +85°C
			179	µA	B model, external clock, −40°C to +125°C
		69	97	µA	B model, external clock, −40°C to +85°C, external reference
			157	µA	B model, external clock, −40°C to +125 °C, external reference
			260	µA	A model, external clock, −40°C to +125°C
Modulator		124	140	µA	B model, external clock, −40°C to +85°C
			193	µA	B model, external clock, −40°C to +125°C
		73	96	µA	B model, external clock, −40°C to +85°C, external reference
			153	µA	B model, external clock, −40°C to +125°C, external reference
			270	µA	A model, external clock, −40°C to +125°C
Crystal Oscillator[3]		33	60	µA	External crystal, 16 pF at XTAL1 and XTAL2
		44	71	µA	External crystal, 36 pF at XTAL1 and XTAL2
Internal Oscillator[4]		218	285	µA	AD5700-1 only, external crystal not required
Power-Down Mode					$\overline{RESET}$ = REF_EN = DGND
V_{CC} and IOV_{CC} Current Consumption		16	35	µA	Internal reference disabled, −40°C to +85°C
			75	µA	Internal reference disabled, −40°C to +125°C
INTERNAL VOLTAGE REFERENCE					
Internal Reference Voltage	1.47	1.5	1.52	V	REF_EN = IOV_{CC} to enable use of internal reference
Load Regulation		18		ppm/µA	Tested with 50 µA load
OPTIONAL EXTERNAL VOLTAGE REFERENCE					
External Reference Input Voltage	2.47	2.5	2.53	V	REF_EN = DGND to enable use of external reference, V_{CC} = 2.7 V minimum
External Reference Input Current					
Demodulator		16	21	µA	Current required by external reference in receive mode
Modulator		28	33	µA	Current required by external reference in transmit mode
Internal Oscillator		5.5	7	µA	Current required by external reference if using internal oscillator
Power-Down		4.6	8.6	µA	
DIGITAL INPUTS					
V_{IH}, Input High Voltage	0.7 × IOV_{CC}			V	
V_{IL}, Input Low Voltage			0.3 × IOV_{CC}	V	
Input Current	−0.1		+0.1	µA	
Input Capacitance[5]		5		pF	Per pin

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DIGITAL OUTPUTS					
V_{OH}, Output High Voltage	IOV_{CC} − 0.5			V	
V_{OL}, Output Low Voltage			0.4	V	
CD Assert[6]	85	100	110	mV p-p	
HART_IN INPUT[5]					
Input Voltage Range	0		REF	V	External reference source
	0		1.5	V	Internal reference enabled
HART_OUT OUTPUT					
Output Voltage	459	493	505	mV p-p	AC-coupled (2.2 µF), measured at HART_OUT pin with 160 Ω load (worst-case load), see Figure 15 and Figure 16 for HART_OUT voltage vs. load
Mark Frequency[7]		1200		Hz	Internal oscillator
Space Frequency[7]		2200		Hz	Internal oscillator
Frequency Error	−0.5		+0.5	%	Internal oscillator, −40°C to +85°C
	−1		+1	%	Internal oscillator, −40°C to +125°C
Phase Continuity Error[5]			0	Degrees	
Maximum Load Current[5]		160		Ω	Worst-case load is 160 Ω, ac-coupled with 2.2 µF, see Figure 19 for recommended configuration if driving a resistive load
Transmit Impedance		7		Ω	$\overline{RTS}$ low, at the HART_OUT pin
		70		kΩ	$\overline{RTS}$ high, at the HART_OUT pin

[1] Temperature range: −40°C to +125°C; typical at 25°C.
[2] Current consumption specifications are based on mean current values.
[3] The demodulator and modulator currents are specified using an external clock. If using an external crystal oscillator, the crystal oscillator current specification must be added to the corresponding V_{CC} and IOV_{CC} demodulator/modulator current specification to obtain the total supply current required in this mode.
[4] The demodulator and modulator currents are specified using an external clock. If using the internal oscillator, the internal oscillator current specification must be added to the corresponding V_{CC} and IOV_{CC} demodulator/modulator current specification to obtain the total supply current required in this mode.
[5] Guaranteed by design and characterization, but not production tested.
[6] Specification set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 21).
[7] If the internal oscillator is not used, frequency accuracy is dependent on the accuracy of the crystal or clock source used.

TIMING CHARACTERISTICS

V_{CC} = 2 V to 5.5 V, IOV_{CC} = 1.71 V to 5.5 V, T_{MIN} to T_{MAX}, unless otherwise noted, 1 bit time = 1/1200 Hz = 833.333 µs.

Table 3.

Parameter[1]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	1	Bit time[2] max	Carrier start time. Time from $\overline{RTS}$ falling edge to carrier reaching its first peak. See Figure 3.
t_2	1	Bit time[2] max	Carrier stop time. Time from $\overline{RTS}$ rising edge to carrier amplitude dropping to ac zero. See Figure 4.
t_3	1	Bit time[2] max	Carrier decay time. Time from $\overline{RTS}$ rising edge to carrier amplitude dropping to ac zero. See Figure 4.
t_4	6	Bit times[2] max	Carrier detect on. Time from carrier on to CD rising edge. See Figure 5.
t_5	6	Bit times[2] max	Carrier detect off. Time from carrier off to CD falling edge. See Figure 6.
t_6	10	Bit times[2] max	Carrier detect on when switching from transmit mode to receive mode in the presence of a constant valid carrier. Time from $\overline{RTS}$ rising edge to CD rising edge. See Figure 7.
t_7	2.1	ms typ	Crystal oscillator power-up time. On application of a valid power supply voltage at V_{CC} or on enabling of the oscillator via the $\overline{XTAL\_EN}$ pin. Crystal load capacitors = 8 pF.
t_8	6	ms typ	Crystal oscillator power-up time. Crystal load capacitors = 18 pF.
t_9	25	µs typ	Internal oscillator power-up time. On application of a valid power supply voltage at V_{CC} or on enabling of the oscillator via the CLK_CFG0 and CLK_CFG1 pins.
t_{10}	10	ms typ	Reference power-up time.
t_{11}	30	µs typ	Transition time from power-down mode to normal operating mode (external clock source, external reference).

[1] Specifications apply to AD5700/AD5700-1 configured with internal or external receive filter.
[2] Bit time is the length of time to transfer one bit of data.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
V_{CC} to GND	−0.3 V to +7 V
IOV_{CC} to GND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
Digital Output to DGND	−0.3 V to IOV_{CC} + 0.3 V or +7 V (whichever is less)
HART_OUT to AGND	−0.3 V to +2.5 V
HART_IN to AGND	−0.3 V to V_{CC} + 0.3 V or +7 V (whichever is less)
ADC_IP	−0.3 V to V_{CC} + 0.3 V or +7 V (whichever is less)
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	150°C
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
Lead Temperature,	JEDEC industry standard
Soldering	J-STD-020
ESD	
Human Body Model (ANSI/ESDA/JEDEC JS-001-2010)	8 kV
Field Induced Charge Model (JEDEC JESD22_C101E)	1.5 kV
Machine Model (ANSI/ESD S5.2-2009)	400 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
24-Lead LFCSP	30	3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

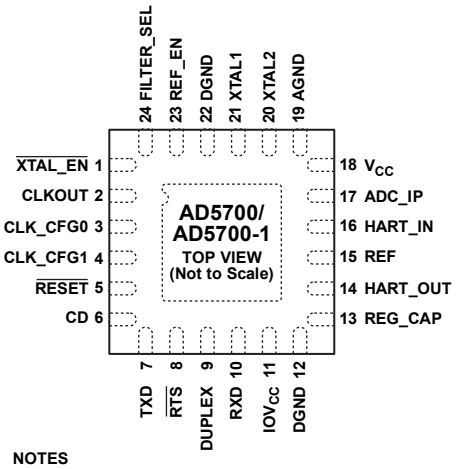

Figure 2. AD5700/AD5700-1 Pin Configuration

Table 6. AD5700/AD5700-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{XTAL\_EN}}$	Crystal Oscillator Circuit Enable. A low state enables the crystal oscillator circuit, and an external crystal is required. A high state disables the crystal oscillator circuit, and an external clock source or the internal oscillator (AD5700-1 only) provides the clock source. This pin is used in conjunction with the CLK_CFG0 and CLK_CFG1 pins in configuring the required clock generation scheme.
2	CLKOUT	Clock Output. If using the crystal oscillator or the internal RC oscillator, a clock output can be configured at the CLKOUT pin. Enabling the clock output consumes extra current to drive the load on this pin. See the CLKOUT section for more details.
3	CLK_CFG0	Clock Configuration Control. See Table 7.
4	CLK_CFG1	Clock Configuration Control. See Table 7.
5	$\overline{\text{RESET}}$	Active Low Digital Input. Holding $\overline{\text{RESET}}$ low places the AD5700/AD5700-1 in power-down mode. A high state on $\overline{\text{RESET}}$ returns the AD5700/AD5700-1 to their power-on state. If not using this pin, tie this pin to IOV_{CC}.
6	CD	Carrier Detect—Digital Output. A high on CD indicates a valid carrier is detected.
7	TXD	Transmit Data—Digital Input. Data input to the modulator.
8	$\overline{\text{RTS}}$	Request to Send—Digital Input. A high state enables the demodulator and disables the modulator. A low state enables the modulator and disables the demodulator.
9	DUPLEX	A high state on this pin enables full duplex operation. See the Theory of Operation section. A low state disables this feature.
10	RXD	Receive Data—UART Interface Digital Data Output. Data output from the demodulator is accessed on this pin.
11	IOV_{CC}	Digital Interface Supply. Digital threshold levels are referenced to the voltage applied to this pin. The applied voltage can be in the range of 1.71 V to 5.5 V.
12	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
13	REG_CAP	Capacitor Connection for Internal Voltage Regulator. Connect a 1 µF capacitor from this pin to ground.
14	HART_OUT	HART FSK Signal Output. See the FSK Modulator section and Figure 26 for typical connections.
15	REF	Internal Reference Voltage Output, or External 2.5 V Reference Voltage Input. Connect a 1 µF capacitor from this pin to ground. When supplying an external reference, the V_{CC} supply requires a minimum voltage of 2.7 V.
16	HART_IN	HART FSK Signal. When using the internal filter, couple the HART input signal into this pin using a 2.2 nF series capacitor. If using an external band-pass filter as shown in Figure 21, do not connect to this pin.
17	ADC_IP	If using the internal band-pass filter, connect 680 pF to this pin. Alternatively, this pin allows direct connection to the ADC input, in which case an external band-pass filter network must be used, as shown in Figure 21.
18	V_{CC}	Power Supply Input. 2 V to 5.5 V can be applied to this pin. V_{CC} should be decoupled to ground with low ESR 10 µF and 0.1 µF capacitors (see the Supply Decoupling section).
19	AGND	Analog Circuitry Ground Reference Connection.

Pin No.	Mnemonic	Description
20	XTAL2	Connection for External 3.6864 MHz Crystal. Do not connect to this pin if using the internal RC oscillator (AD5700-1 only) or an external clock source.
21	XTAL1	Connection for External 3.6864 MHz Crystal or External Clock Source Input. Tie this pin to ground if using the internal RC oscillator (AD5700-1 only).
22	DGND	Digital Circuitry Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.
23	REF_EN	Reference Enable. A high state enables the internal 1.5 V reference and buffer. A low state disables the internal reference and input buffer, and a buffered external 2.5 V reference source must be applied at REF. If REF_EN is tied low, V_{CC} must be greater than 2.7 V.
24	FILTER_SEL	Band-Pass Filter Select. A high state enables the internal filter and the HART signal should be applied to the HART_IN pin. A low state disables the internal filter and an external band-pass filter must then be connected at the ADC_IP input pin. In this case, the HART signal should be applied to the ADC_IP pin.
EPAD	AGND	Analog Ground Reference Connection. For typical operation, it is recommended to connect this pin to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

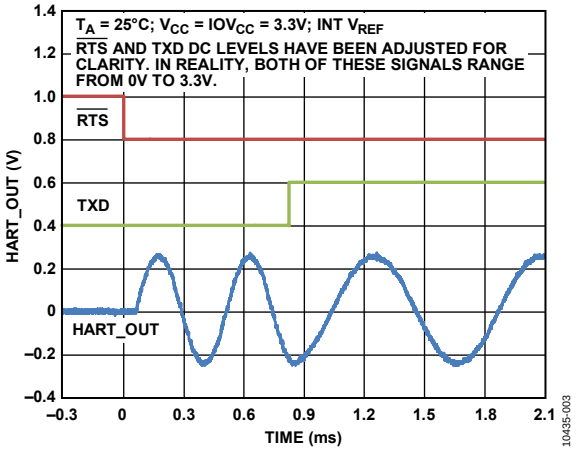

Figure 3. Carrier Start Time

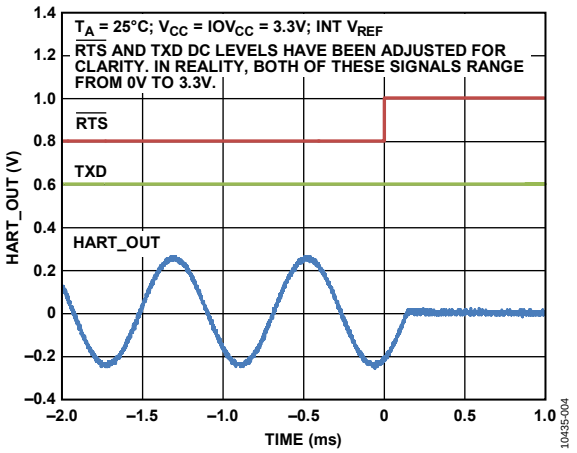

Figure 4. Carrier Stop/Decay Time

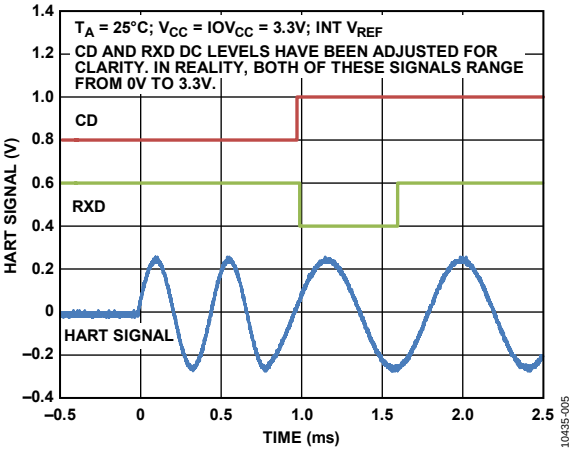

Figure 5. Carrier Detect On Timing

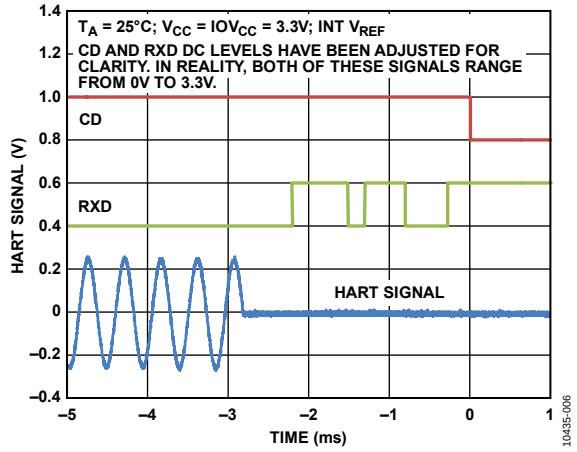

Figure 6. Carrier Detect Off Timing

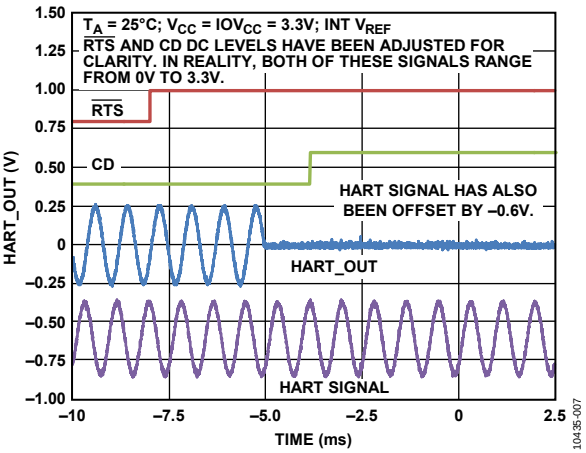

Figure 7. Carrier Detect on When Switching from Transmit Mode to Receive Mode in the Presence of a Constant Valid Carrier

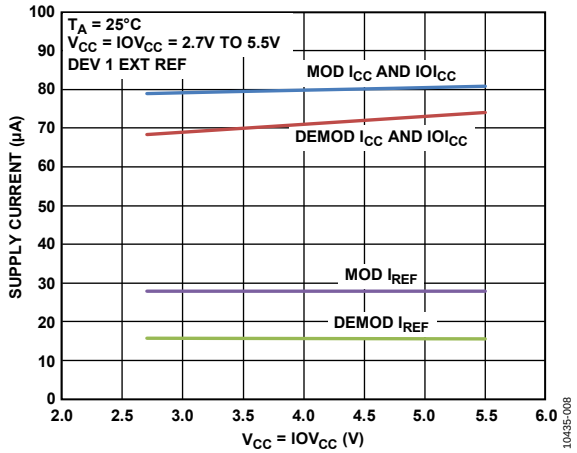

Figure 8. Supply Currents vs. Supply Voltage—External Reference

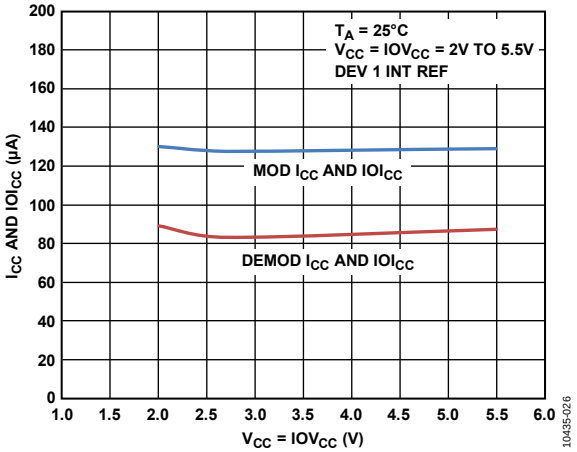

Figure 9. Supply Currents vs. Supply Voltage—Internal Reference

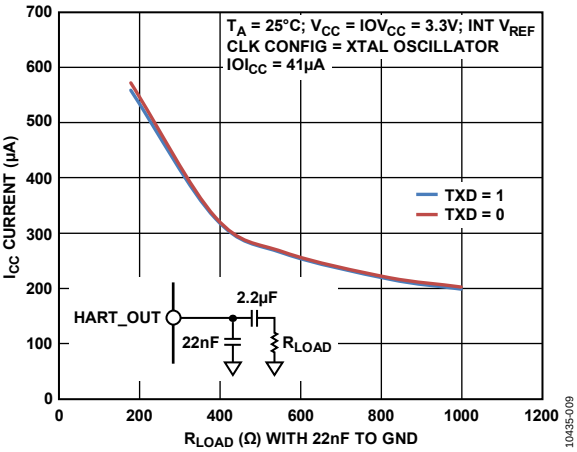

Figure 10. Current in Tx Mode vs. Resistive Load

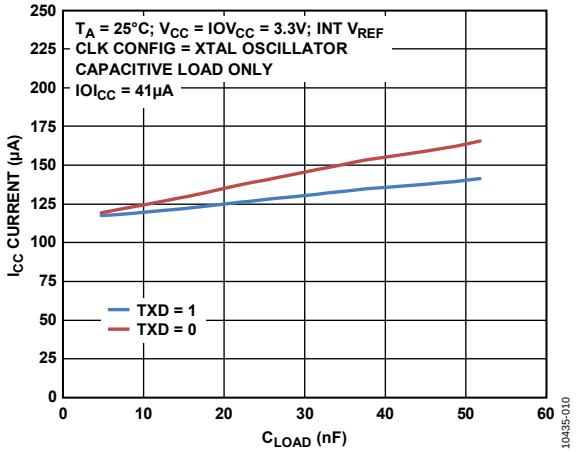

Figure 11. Current in Tx Mode vs. Capacitive Load

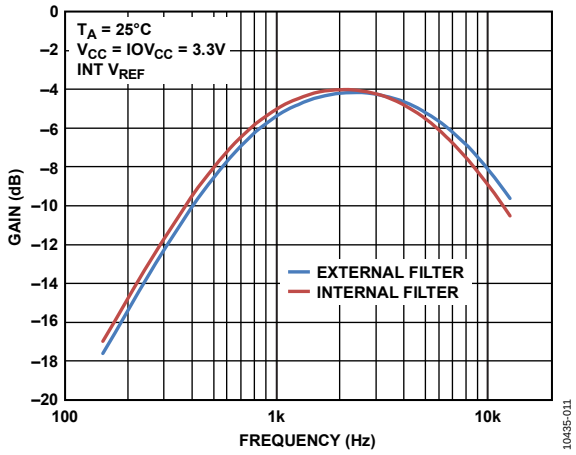

Figure 12. Input Filter Frequency Response

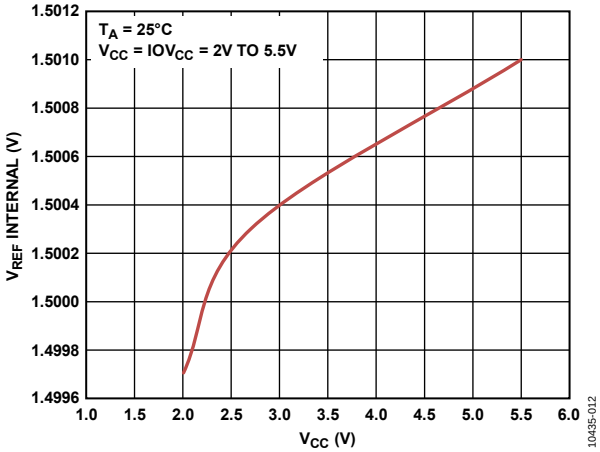

Figure 13. Reference Voltage vs. V_{CC}

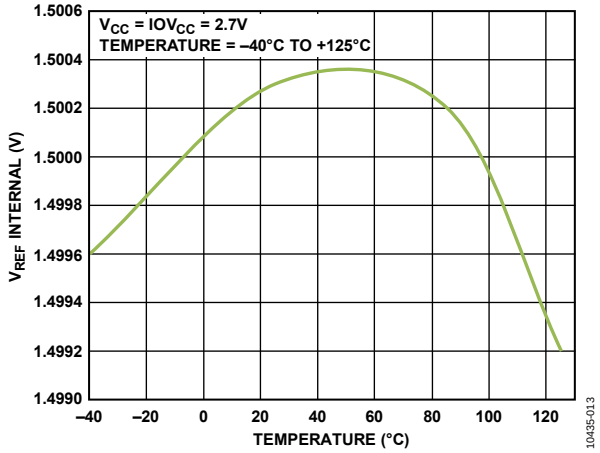

Figure 14. Reference Voltage vs. Temperature

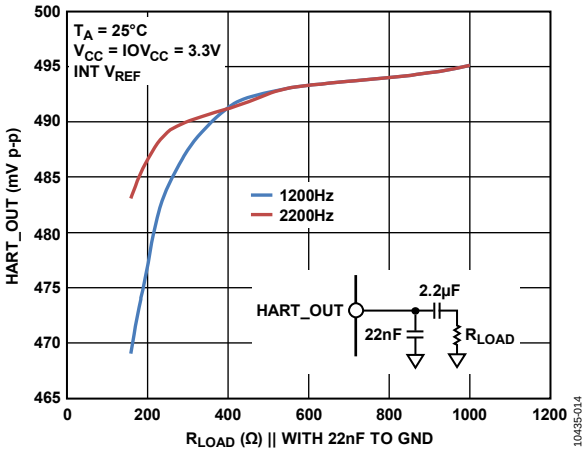

Figure 15. HART_OUT Voltage vs. R_{LOAD}

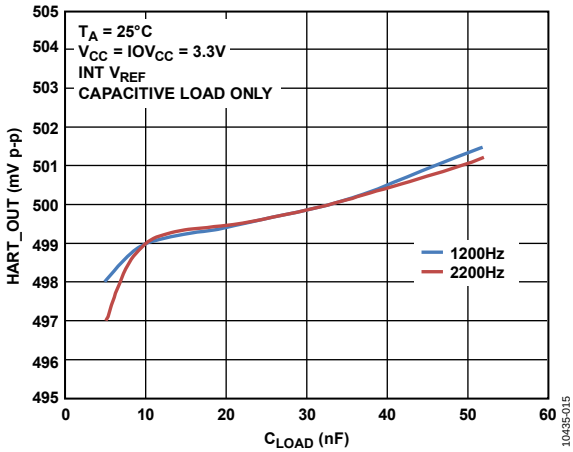

Figure 16. HART_OUT Voltage vs. C_{LOAD}

TERMINOLOGY

V_{CC} and IOV_{CC} Current Consumption
This specification gives a summation of the current consumption of both the V_{CC} and the IOV_{CC} supplies. Figure 11 shows separate measurements for V_{CC} and IOV_{CC} currents vs. varying capacitive loads, in transmit mode.

Load Regulation
Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/μA.

CD Assert
The minimum value at which the carrier detect signal asserts is 85 mV p-p and the maximum value it asserts at is 110 mV p-p. CD is already high (asserted) for HART input signals greater than 110 mV p-p. This specification was set assuming a sinusoidal input signal containing preamble characters at the input and an ideal external filter (see Figure 21).

HART_OUT Output Voltage
This is the peak-to-peak HART_OUT output voltage. The specification in Table 2 was set using a worst-case load of 160 Ω, ac-coupled with a 2.2 μF capacitor. Figure 15 and Figure 16 show HART_OUT output voltages for both resistive and purely capacitive loads.

Mark/Space Frequency
A 1.2 kHz signal represents a digital 1, or mark, whereas a 2.2 kHz signal represents a 0, or space.

Phase Continuity Error
The DDS engine in this design inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. This attribute is desirable for signals that are to be transmitted over a band limited channel, because discontinuities in a signal introduce wideband frequency components. As the name suggests, for a signal to be continuous, the phase continuity error must be 0°.

THEORY OF OPERATION

Highway Addressable Remote Transducer (HART) Communication is the global standard for sending and receiving digital information across analog wires between smart field devices and control systems. This is a digital two-way communication system, in which a 1 mA p-p frequency shift keyed (FSK) signal is modulated on top of a 4 mA to 20 mA analog current signal. The AD5700/AD5700-1 are designed and specified to operate as a single-chip, low power, HART FSK half-duplex modem, complying with the HART physical layer requirements (Revision 8.1).

A single-chip solution, the AD5700/AD5700-1 not only integrate the modulation and demodulation functions, but also contain an internal reference, an integrated receive band-pass filter (which has the flexibility of being bypassed if required), and an internally buffered HART output, giving a high output drive capability and removing the need for external buffering. The AD5700-1 option also contains a precision internal RC oscillator. The block diagram in Figure 1 shows a graphical illustration of how these circuit blocks are connected together. As a result of such extensive integration options, minimal external components are required. The AD5700/AD5700-1 are suitable for use in both HART field instrument and master configurations.

The AD5700/AD5700-1 either transmit or receive 1.2 kHz and 2.2 kHz carrier signals. A 1.2 kHz signal represents a digital 1, or mark, whereas a 2.2 kHz signal represents a 0, or space. There are three main clocking configurations supported by these parts, two of which are available on the AD5700 option, whereas all three are available on the AD5700-1 device:

- External crystal
- CMOS clock input
- Internal RC oscillator (AD5700-1 only)

The device is controlled via a standard UART interface. The relevant signals are $\overline{\text{RTS}}$, CD, TXD, and RXD (see Table 6 for more detail on individual pin descriptions).

FSK MODULATOR

The modulator converts a bit stream of UART-encoded HART data at the TXD input to a sequence of 1200 Hz and 2200 Hz tones (see Figure 17). This sinusoidal signal is internally buffered and output on the HART_OUT pin. The modulator is enabled by bringing the $\overline{\text{RTS}}$ signal low.

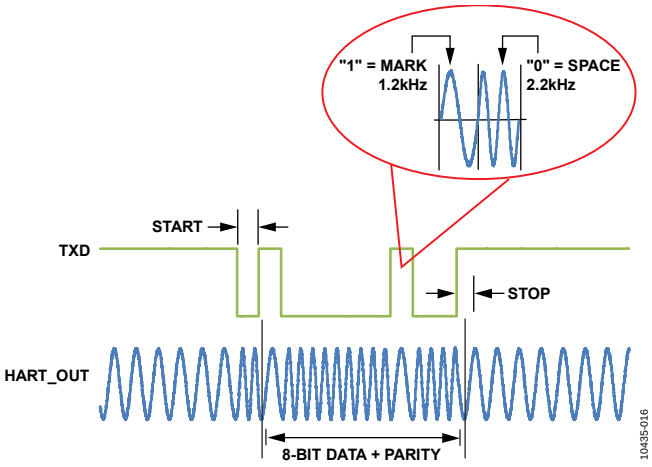

Figure 17. AD5700/AD5700-1 Modulator Waveform

The modulator block contains a DDS engine that produces a 1.2 kHz or 2.2 kHz sine wave in digital form and then performs a digital-to-analog conversion. This DDS engine inherently generates continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. For more information on DDS fundamentals, see MT-085, *Fundamentals of Direct Digital Synthesizers (DDS)*. Figure 18 demonstrates a simple implementation of this FSK encoding.

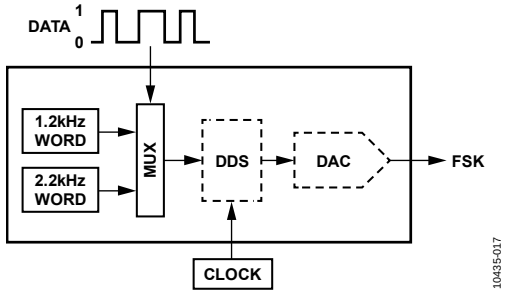

Figure 18. DDS-Based FSK Encoder

CONNECTING TO HART_OUT

The HART_OUT pin is dc biased to 0.75 V and should be capacitively coupled to the load. The current consumption specifications in Table 2 are based on driving a 5 nF load. If the application requires a larger load value, more current is required. This value can be calculated from the following formula:

$$I_{TOTAL} = I_{AD5700} + I_{LOAD\,RMS}$$

$$I_{LOAD\,RMS} = \frac{500\text{ mV}}{4\sqrt{2} \times \sqrt{\left(\frac{1}{2\pi \times f \times C_{LOAD}}\right)^2 + R_{LOAD}{}^2}} \quad (1)$$

where:
I_{AD5700} is the current drawn by the AD5700/AD5700-1 in transmit mode as per specifications (see Table 2). Note that the specifications in Table 2 assume a 5 nF C_{LOAD}.
f is the output frequency (1.2 kHz or 2.2 kHz).
C_{LOAD} is the capacitive load to ground on HART_OUT.
R_{LOAD} is the resistive load on the loop.

When driving a purely capacitive load, the load should be in the range of 5 nF to 52 nF. See Figure 11 for a typical plot of supply current vs. capacitive load.

Example

Assume use of an internal reference, and C_{LOAD} = 52 nF.

I_{CC} + IOI_{CC} = 140 µA maximum (from Table 2 specification)

Note that this is incorporating a 5 nF load.

Therefore, to calculate the load current required to drive the extra 47 nF, use the Equation 1.

Substituting f = 1200 Hz, C_{LOAD} = 47 nF, and R_{LOAD} = 0 Ω into the formula results in I_{LOAD} of 62.6 µA.

If using the crystal oscillator, this adds 60 µA maximum (see Table 2 for conditions).

Thus, the total worst-case current in this example is:

140 µA + 62.6 µA + 60 µA = 262.6 µA

If driving a load with a resistive element, it is recommended to place a 22 nF capacitor to ground at the HART_OUT pin. The load should be coupled with a 2.2 µF series capacitor. For low impedance devices, the R_{LOAD} range is typically 230 Ω to 600 Ω.

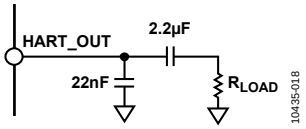

Figure 19. AD5700/AD5700-1 with Resistive Load at HART_OUT

FSK DEMODULATOR

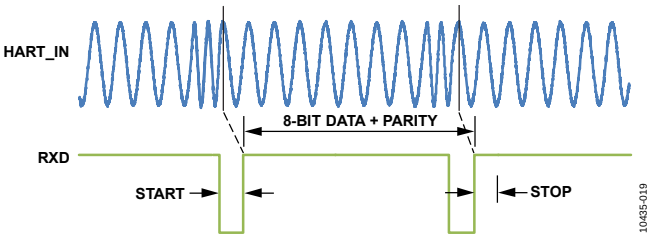

Figure 20. AD5700/AD5700-1 Demodulator Waveform (Preamble Message 0xFF)

When $\overline{RTS}$ is logic high, the modulator is disabled and the demodulator is enabled, that is, the AD5700/AD5700-1 are in receive mode. A high on CD indicates a valid carrier is detected. The demodulator accepts an FSK signal at the HART_IN pin and restores the original modulated signal at the UART interface digital data output pin, RXD. The combination of the ADC, digital filtering and digital demodulation results in a highly accurate output on the RXD pin. The HART bit stream follows a standard UART frame with a start bit, 8-bit data, one parity, and a stop bit (see Figure 20).

CONNECTING TO HART_IN OR ADC_IP

The AD5700/AD5700-1 have two filter configuration options: an external filter (HART signal is applied to ACP_IP) and an internal filter (HART signal is applied to HART_IN).

The external filter configuration is shown in Figure 21. In this case, the HART signal is applied to the ADC_IP pin through an external filter circuit. In safety critical applications, the AD5700/AD5700-1 must be isolated from the high voltage of the loop supply. The recommended external band-pass filter includes a 150 kΩ resistor, which limits current to a sufficiently low level to adhere to intrinsic safety requirements. In this case, the input has higher transient voltage protection and should, therefore, not require additional protection circuitry, even in the most demanding of industrial environments. Assuming the use of a 1% accurate resistor and 10% accurate capacitor components, the calculated variation in CD trip voltage levels vs. the ideal is ±3.5 mV.

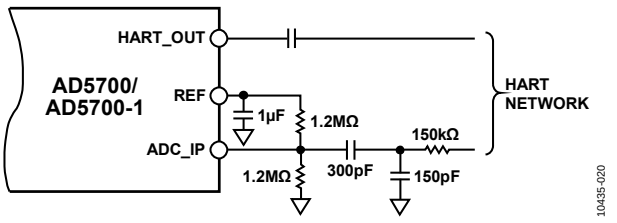

Figure 21. AD5700/AD5700-1 with External Filter on ADC_IP

The internal filter configuration is shown in Figure 22. This option is beneficial where cost or board space is a large concern because it removes the need for multiple external components. This configuration achieves an 8 kV ESD HBM rating but requires extra external protection circuitry for EMC and surge protection purposes if used in harsh industrial environments.

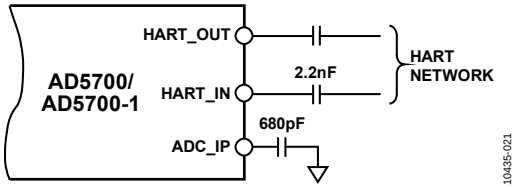

Figure 22. AD5700/AD5700-1 Using Internal Filter on HART_IN

CLOCK CONFIGURATION

The AD5700/AD5700-1 support numerous clocking configurations to allow the optimal trade-off between cost and power:

- External crystal
- CMOS clock input
- Internal RC oscillator (AD5700-1 only)

The CLK_CFG0, CLK_CFG1, and $\overline{\text{XTAL\_EN}}$ pins configure the clock generation as shown in Table 7. The AD5700/AD5700-1 can also provide a clock output at CLKOUT (for more details, see the CLKOUT section).

External Crystal

The typical connection for an external crystal (ABLS-3.6864MHZ-L4Q-T) is shown in Figure 23. To ensure minimum current consumption and to minimize stray capacitances, connections between the crystal, capacitors, and ground should be made as close to the AD5700/AD5700-1 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

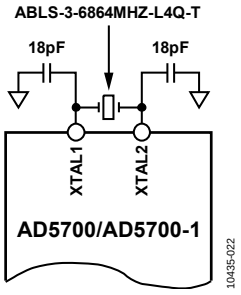

Figure 23. Crystal Oscillator Connection

The ABLS-3.6864MHZ-L4Q-T crystal oscillator data sheet recommended two 18 pF capacitors. Because the crystal current consumption is dominated by the load capacitance, in an effort to reduce the crystal current consumption, two 8 pF capacitors were used on the XTAL1 and XTAL2 pins. The AD5700/AD5700-1 still functioned as expected, even with the resulting reduction in frequency performance from the crystal due to the smaller capacitance values. Crystals are available that support 8 pF capacitors. It is recommended to consult the relevant crystal manufacturers for this information.

CMOS Clock Input

A CMOS clock input can also be used to generate a clock for the AD5700/AD5700-1. To use this mode, connect an external clock source to the XTAL 1 pin, and leave XTAL2 open circuit (see Figure 24).

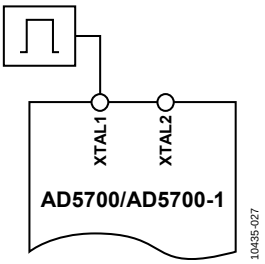

Figure 24. CMOS Clock Connection

Internal Oscillator (AD5700-1 only)

Consuming typically 218 µA, the low power, internal, 0.5 % precision RC oscillator, available only on the AD5700-1, has an oscillation frequency of 1.2288 MHz. To use this mode, tie the XTAL1 pin to ground and leave the XTAL2 pin open circuit (see Figure 25).

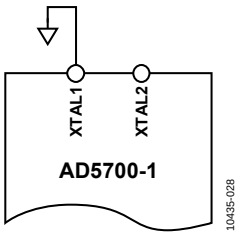

Figure 25. Internal Oscillator Connection

CLKOUT

The AD5700/AD5700-1 can provide a clock output at CLKOUT (see Table 7).

- If using the crystal oscillator, this clock output can be configured as a 3.6864 MHz, 1.8432 MHz, or 1.2288 MHz buffer clock.
- If using a CMOS clock, no clock output can be configured at the CLKOUT pin.
- If using the internal RC oscillator, this clock output is only available as a 1.2288 MHz buffer clock.

The amplitude of the clock output depends on the IOV_{CC} level; therefore, the clock output can be in the range of 1.71 V p-p to 5.5 V p-p. Enabling the clock output of the AD5700/AD5700-1 increases the current consumption of the device. This increase is due to the current required to drive any load at the CLKOUT pin, which should not be more than 30 pF.

This capacitance should be minimized to reduce current consumption and provide the clock with the cleanest edges. The additional current drawn from the IOV_{CC} supply can be calculated using the following equation:

$$I = C \times V \times f$$

Table 7. Clock Configuration Options

$\overline{\text{XTAL\_EN}}$	CLK_CFG1	CLK_CFG0	CLKOUT	Description
1	0	0	No output	3.6864 MHz CMOS clock connected at XTAL1 pin
1	0	1	No output	1.2288 MHz CMOS clock connected at XTAL1 pin
1	1	0	No output	Internal oscillator enabled (AD5700-1 only)
1	1	1	1.2288 MHz output	Internal oscillator enabled, CLKOUT enabled (AD5700-1 only)
0	0	0	No output	Crystal oscillator enabled
0	0	1	3.6864 MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	0	1.8432 MHz output	Crystal oscillator enabled, CLKOUT enabled
0	1	1	1.2288 MHz output	Crystal oscillator enabled, CLKOUT enabled

POWER-DOWN MODE

The AD5700/AD5700-1 can be placed into power-down mode by holding the $\overline{\text{RESET}}$ pin low. If using the internal reference, it is recommended to tie the REF_EN pin to the $\overline{\text{RESET}}$ pin so that it is also powered down. If the reference is not powered down while $\overline{\text{RESET}}$ is low, the output voltage on the REF pin is approximately 1.7 V until $\overline{\text{RESET}}$ is brought high again.

In this mode, the receive, transmit, and oscillator circuits are all switched off, and the device consumes a typical current of 16 μA.

FULL DUPLEX OPERATION

Full duplex operation means that the modulator and demodulator of the AD5700/AD5700-1 are enabled at the same time. This is a powerful feature, enabling a self-test procedure of not only the HART device but also the complete signal path between the HART device and the host controller. This provides verification that the local communications loop is functional. This increased level of system diagnostics is useful in production self-test and is advantageous in improving the application's safety integrity level (SIL) rating. The full duplex mode of operation is enabled by connecting the DUPLEX pin to logic high.

APPLICATIONS INFORMATION

SUPPLY DECOUPLING

It is recommended to decouple the V_{CC} and IOV_{CC} supplies with 10 µF in parallel with 0.1 µF capacitors to ground. For many applications, 1 µF in parallel with 0.1 µF ceramic capacitors to ground should be sufficient. The REG_CAP voltage of 1.8 V is used to supply the AD5700/AD5700-1 internal circuitry and is derived from the V_{CC} supply using a high efficiency clocking LDO. Decouple this REG_CAP supply with a 1 µF ceramic capacitor to ground. It is also required to decouple the REF pin with a 1 µF ceramic capacitor to ground. Place decoupling capacitors as close to the relevant pins as possible.

For loop-powered applications, it is recommended to connect a resistance in series with the V_{CC} supply to minimize the effect of any noise, which may, depending on the system configuration, be introduced onto the loop as a result of current draw variations from the AD5700/AD5700-1. For typical applications, 470 Ω of resistance has proven most effective. However, depending on the application conditions, alternative values may also be acceptable (see R1 in Figure 27).

TYPICAL CONNECTION DIAGRAMS

Figure 26 shows a typical connection diagram for the AD5700/AD5700-1 using the external and internal options. See the Connecting to HART_IN or ADC_IP section for more details.

The AD5700/AD5700-1 are designed to interface easily with Analog Devices, Inc., innovative portfolio of industrial converters like the AD5421 loop-powered current-output DAC, the AD5410/AD5420 and AD5412/AD5422 family of line-powered current-output DACs, and the AD5755-1, a quad DAC with innovative dynamic power control technology. The combination of Analog Devices industrial converters and the AD5700/AD5700-1 greatly simplifies system design, enhancing reliability while reducing overall PCB size.

Figure 27 shows how the AD5700/AD5700-1 HART modem can be interfaced with the AD5421 (4 mA to 20 mA loop-powered DAC) and a microcontroller to construct a loop powered transmitter circuit. The HART signal from HART_OUT is introduced to the AD5421 via the C_{IN} pin.

The HART enabled smart transmitter reference demo circuit (the block diagram shown in Figure 28) was developed by Analog Devices and uses the AD5421, a 16-bit, loop-powered, 4 mA to 20 mA DAC, and the AD5700 modem. This circuit has been compliance tested, verified, and registered as an approved HART solution by the HART Communication Foundation. Contact your sales representative for further information about this demo circuit.

In conclusion, the AD5700/AD5700-1 enable quick and easy deployment of a robust HART-compliant system.

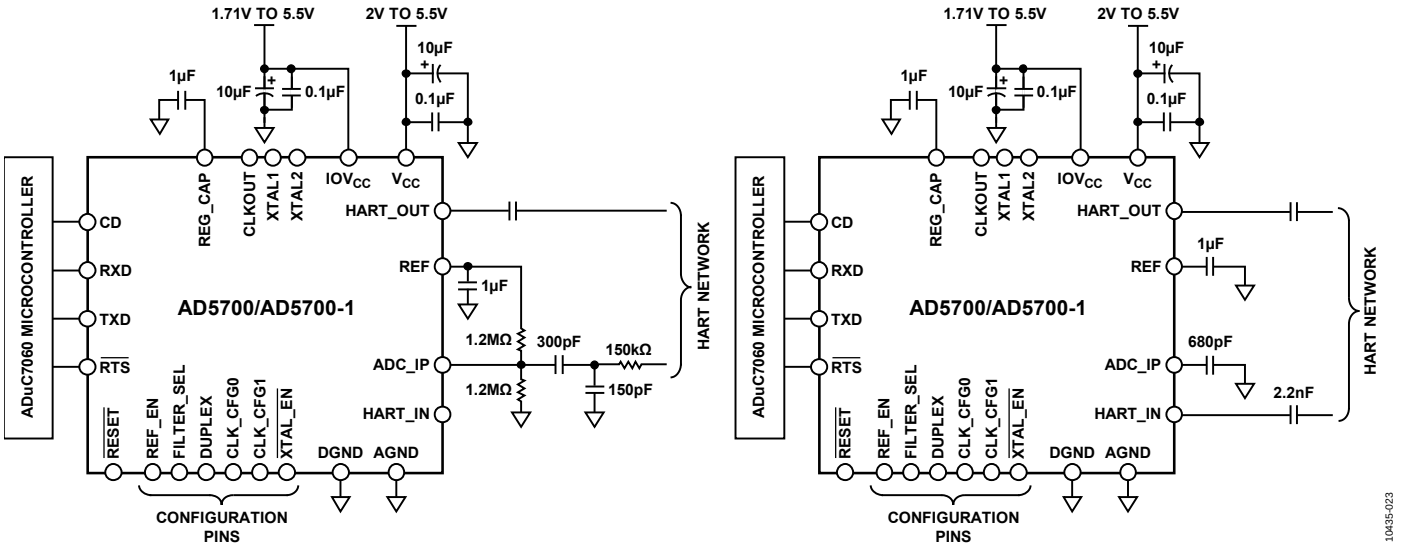

Figure 26. AD5700/AD5700-1 Typical Connection Diagram for External and Internal Filter Options

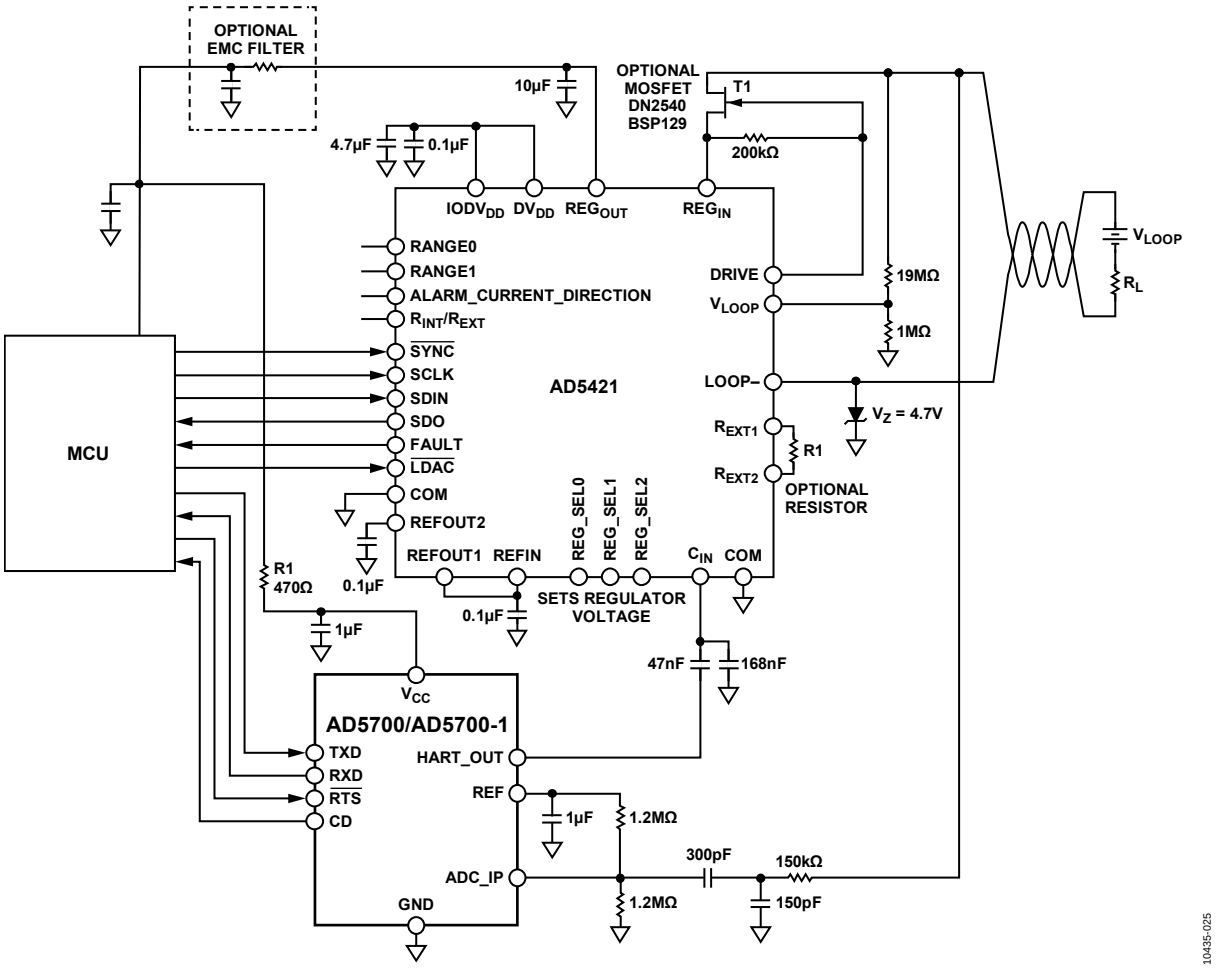

Figure 27. Loop-Powered Transmitter Diagram

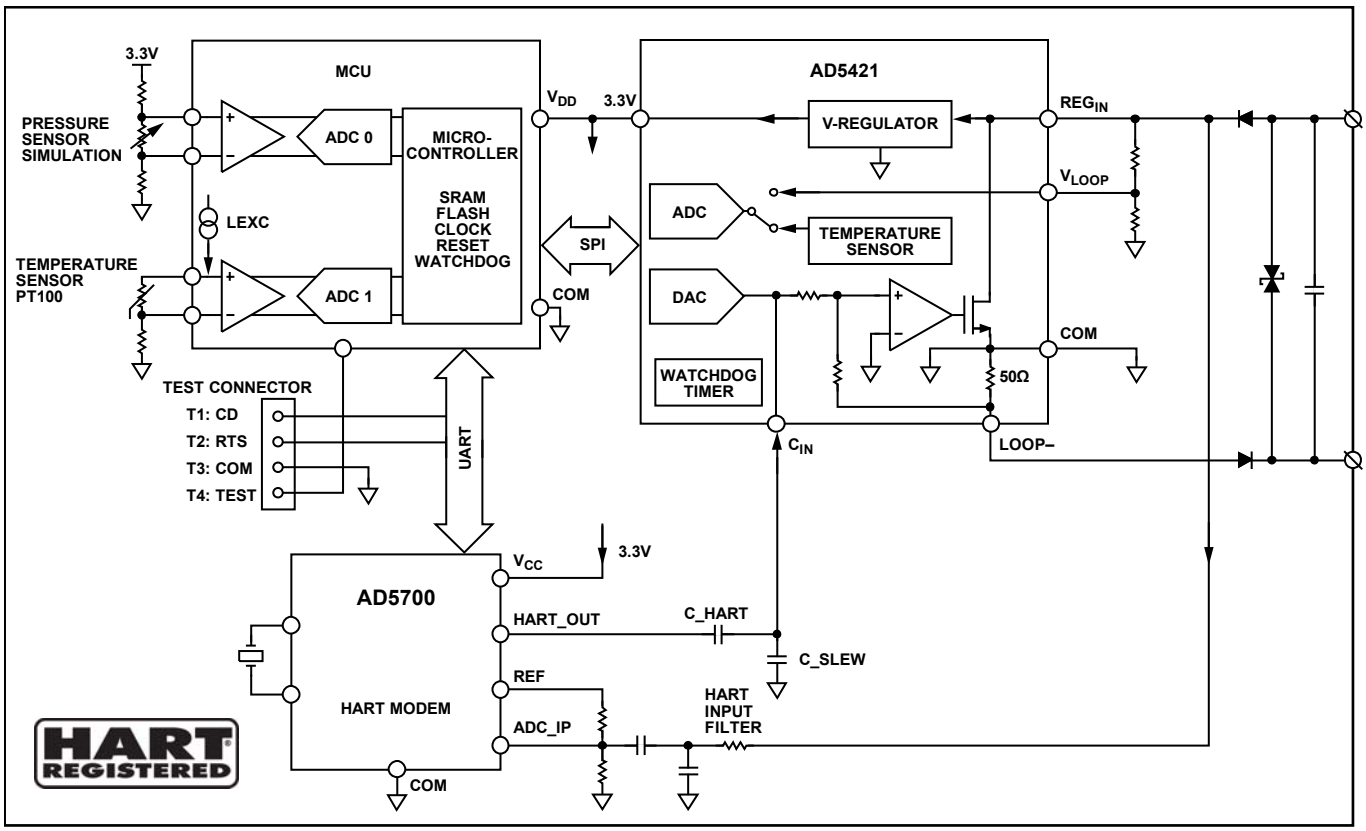

Figure 28. Block Diagram—Analog Devices HART-Enabled Smart Transmitter Reference Demo Circuit

OUTLINE DIMENSIONS

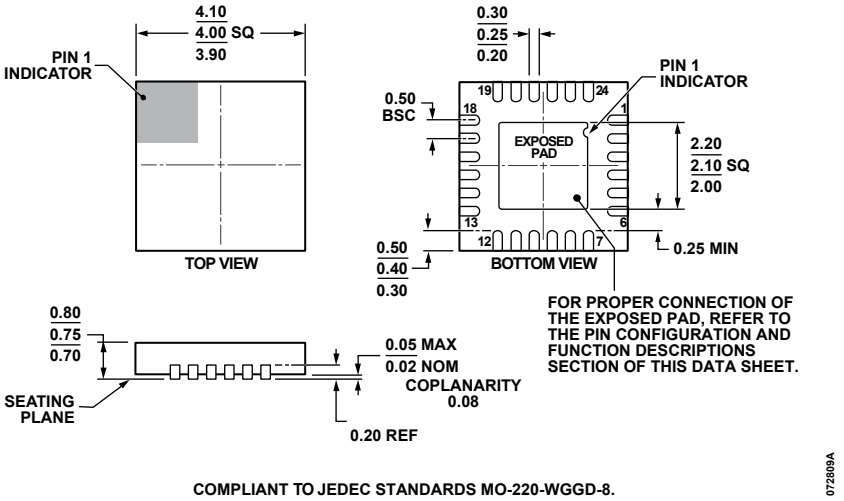

Figure 29. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Oscillator Options	Receive Supply Current	Package Description	Package Option
AD5700BCPZ-R5	−40°C to +125°C	External clock, crystal	157 µA	24-Lead LFCSP_WQ	CP-24-10
AD5700BCPZ-RL7	−40°C to +125°C	External clock, crystal	157 µA	24-Lead LFCSP_WQ	CP-24-10
AD5700ACPZ-RL7	−40°C to +125°C	External clock, crystal	260 µA	24-Lead LFCSP_WQ	CP-24-10
AD5700-1BCPZ-R5	−40°C to +125°C	External clock, crystal or internal oscillator	442 µA	24-Lead LFCSP_WQ	CP-24-10
AD5700-1BCPZ-RL7	−40°C to +125°C	External clock, crystal or internal oscillator	442 µA	24-Lead LFCSP_WQ	CP-24-10
AD5700-1ACPZ-RL7	−40°C to +125°C	External clock, crystal or internal oscillator	540 µA	24-Lead LFCSP_WQ	CP-24-10
EVAL-AD5700-1EBZ				Evaluation Board for AD5700 and AD5700-1	

[1] Z = RoHS Compliant Part.