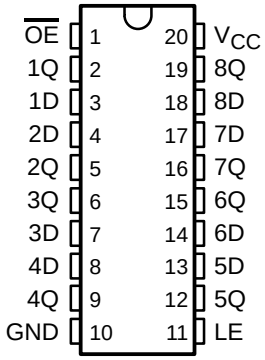
- **Eight High-Current Latches in a Single Package**
- **High-Current 3-State True Outputs Can Drive up to 15 LSTTL Loads**
- **Full Parallel Access for Loading**

DB, N, OR PW PACKAGE
(TOP VIEW)



description

This 8-bit latch features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the SN74HC373A are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable ($\overline{OE}$) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

ORDERING INFORMATION

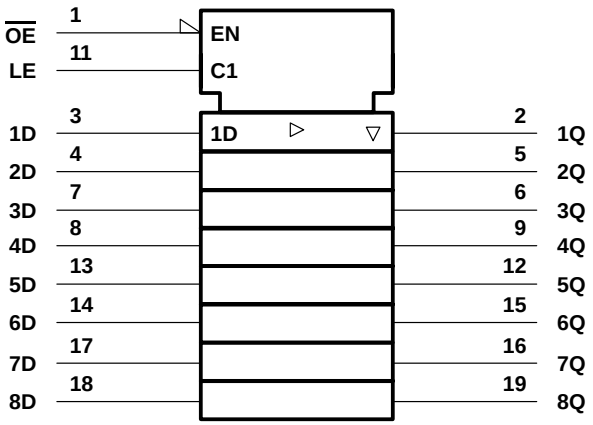
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74HC373AN	SN74HC373AN
	SSOP – DB	Tape and reel	SN74HC373ADBR	HC373A
	TSSOP – PW	Tape and reel	SN74HC373APWR	HC373A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

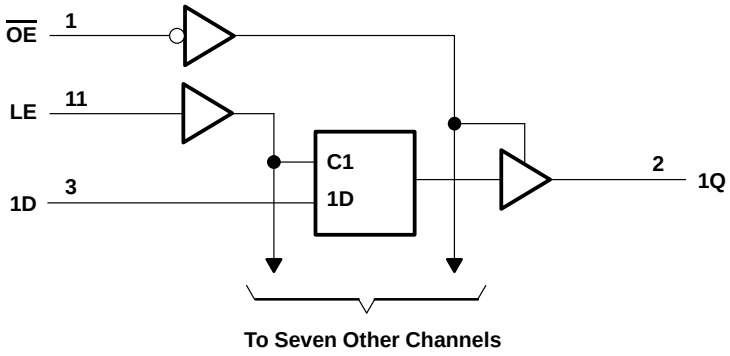
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . . 70°C/W
N package . . . . . 69°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 6 V	4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	
		V_{CC} = 6 V	0		1.8	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	ns
		V_{CC} = 4.5 V	0		500	
		V_{CC} = 6 V	0		400	
T_A	Operating free-air temperature		–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		V
			4.5 V	4.4	4.499		4.4		
			6 V	5.9	5.999		5.9		
		I_{OH} = –6 mA	4.5 V	3.98	4.3		3.84		
		I_{OH} = –7.8 mA	6 V	5.48	5.8		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			6 V			0.1		0.1	
		I_{OL} = 6 mA	4.5 V			0.26		0.33	
		I_{OL} = 7.8 mA	6 V			0.26		0.33	
I_I	V_I = V_{CC} or 0		6 V		±0.1	±100		±1000	nA
I_{OZ}	V_O = V_{CC} or 0		6 V			±0.5		±5	μA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		80	μA
C_i			2 V to 6 V		3	10		10	pF

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
t_w	Pulse duration, LE high	2 V	75		95		ns
		4.5 V	15		19		
		6 V	13		16		
t_{su}	Setup time, data before LE↓	2 V	50		63		ns
		4.5 V	10		13		
		6 V	9		11		
t_h	Hold time, data after LE↓	2 V	20		24		ns
		4.5 V	10		12		
		6 V	10		12		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D	Q	2 V		55	125		155	ns
			4.5 V		15	25		31	
			6 V		12	21		26	
	LE	Any Q	2 V		71	125		155	
			4.5 V		20	25		31	
			6 V		16	21		26	
t_{en}	$\overline{OE}$	Any Q	2 V		60	125		155	ns
			4.5 V		17	25		31	
			6 V		13	21		26	
t_{dis}	$\overline{OE}$	Any Q	2 V		44	125		155	ns
			4.5 V		19	25		31	
			6 V		17	21		26	
t_t		Any Q	2 V		22	60		75	ns
			4.5 V		7	12		15	
			6 V		5	10		13	

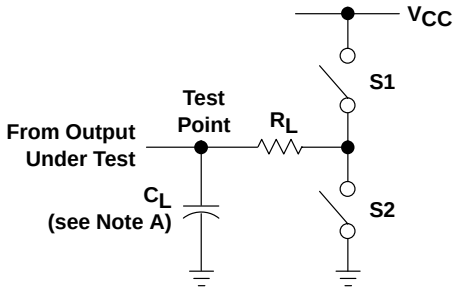
switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{pd}	D	Q	2 V		73	175		220	ns
			4.5 V		20	35		44	
			6 V		16	30		37	
	LE	Any Q	2 V		90	175		220	
			4.5 V		25	35		44	
			6 V		20	30		37	
t_{en}	$\overline{OE}$	Any Q	2 V		78	175		220	ns
			4.5 V		21	35		44	
			6 V		17	30		37	

operating characteristics, T_A = 25°C

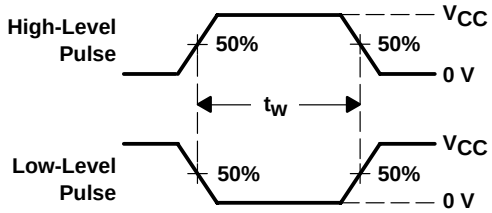
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	100	pF

PARAMETER MEASUREMENT INFORMATION

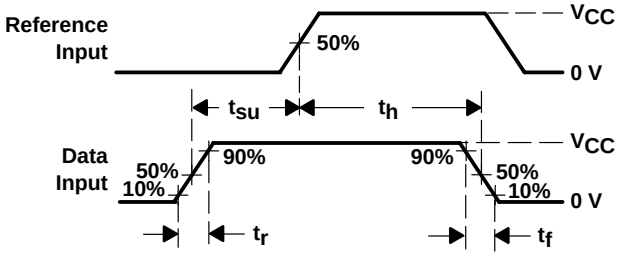


LOAD CIRCUIT

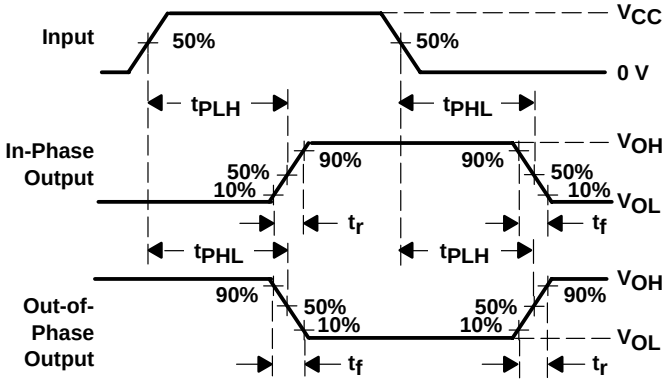
PARAMETER		R_L	C_L	S1	S2
t_{en}	t_{PZH}	1 kΩ	50 pF or 150 pF	Open	Closed
	t_{PZL}			Closed	Open
t_{dis}	t_{PHZ}	1 kΩ	50 pF	Open	Closed
	t_{PLZ}			Closed	Open
t_{pd} or t_t		––	50 pF or 150 pF	Open	Open



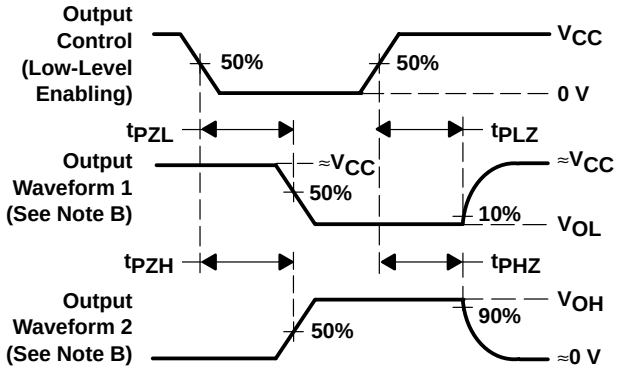
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265