

Features

- 100V/120A,
 $R_{DS(ON)} = 7m\Omega(Typ.)@V_{GS}=10V$
- Low $R_{DS(ON)}$
- Super High Dense Cell Design
- Reliable and Rugged
- 100% Avalanche Tested

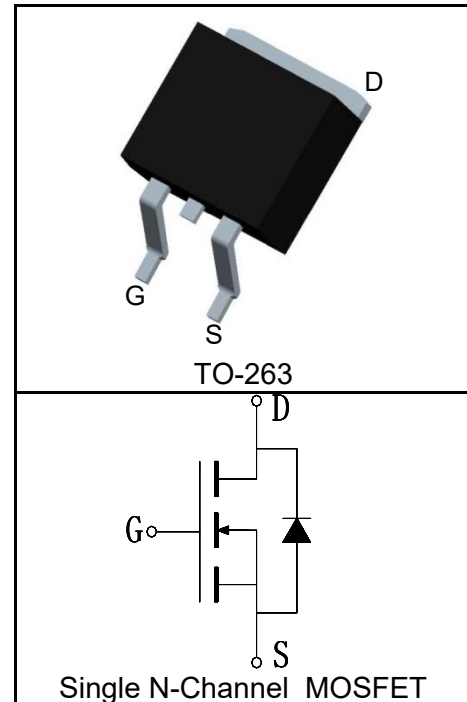
Applications

- DC-DC Converters and Off-line UPS
- Power Management in Inverter System



Halogen-Free

Pin Description



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
Common Ratings ($T_C=25^\circ\text{C}$ Unless Otherwise Noted)			
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
I_S	Diode Continuous Forward Current	$T_C=25^\circ\text{C}$ 120	A
Mounted on Large Heat Sink			
$I_{DP}^{(1)}$	300 μs Pulse Drain Current Tested	$T_C=25^\circ\text{C}$ 480	A
$I_D^{(2)}$	Continuous Drain Current($V_{GS}=10V$)	$T_C=25^\circ\text{C}$ 120	A
		$T_C=100^\circ\text{C}$ 76	
P_D	Maximum Power Dissipation	$T_C=25^\circ\text{C}$ 192	W
		$T_C=100^\circ\text{C}$ 76	
$R_{\theta JC}$	Thermal Resistance-Junction to Case	0.65	$^\circ\text{C/W}$
$R_{\theta JA}^{(3)}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C/W}$
Drain-Source Avalanche Ratings			
$E_{AS}^{(4)}$	Avalanche Energy, Single Pulsed	992	mJ

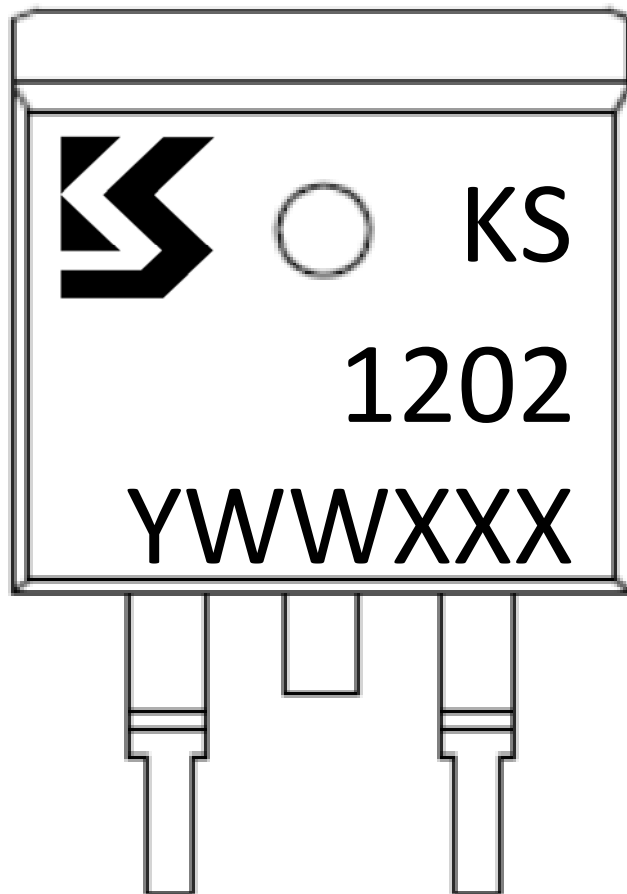
Electrical Characteristics ($T_C=25^{\circ}\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Test Condition	KS1202GA			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V			1	μA
			T _J =125°C		30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	2		4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V			±100	nA
R _{DS(ON)} ^⑤	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =40A		7	8	mΩ
Diode Characteristics						
V _{SD} ^⑤	Diode Forward Voltage	I _{SD} =40A, V _{GS} =0V		0.84	1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} =40A, dI _{SD} /dt=100A/μs		53		ns
Q _{rr}	Reverse Recovery Charge			136		nC
Dynamic Characteristics ^⑥						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz		2.6		Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, Frequency=1.0MHz		6825		pF
C _{oss}	Output Capacitance			500		
C _{rss}	Reverse Transfer Capacitance			345		
t _{d(ON)}	Turn-on Delay Time	V _{DD} =50V, I _{DS} =1A, V _{GEN} =10V, R _G =6Ω		33		ns
t _r	Turn-on Rise Time			59		
t _{d(OFF)}	Turn-off Delay Time			86		
t _f	Turn-off Fall Time			29		
Gate Charge Characteristics ^⑥						
Q _g	Total Gate Charge	V _{DS} =80V, V _{GS} =10V, I _{DS} =40A		146		nC
Q _{gs}	Gate-Source Charge			30		
Q _{gd}	Gate-Drain Charge			60		

- Notes:
- ① Pulse width limited by safe operating area.
 - ② Calculated continuous current based on maximum allowable junction temperature. The package limitation current is 75A.
 - ③ When mounted on 1 inch square copper board, $t \leq 10\text{sec}$. The value in any given application depends on the user's specific board design.
 - ④ Limited by T_{Jmax} , $I_{AS}=63A$, $L=0.5\text{mH}$, $V_{DD}=48V$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$.
 - ⑤ Pulse test; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 - ⑥ Guaranteed by design, not subject to production testing.

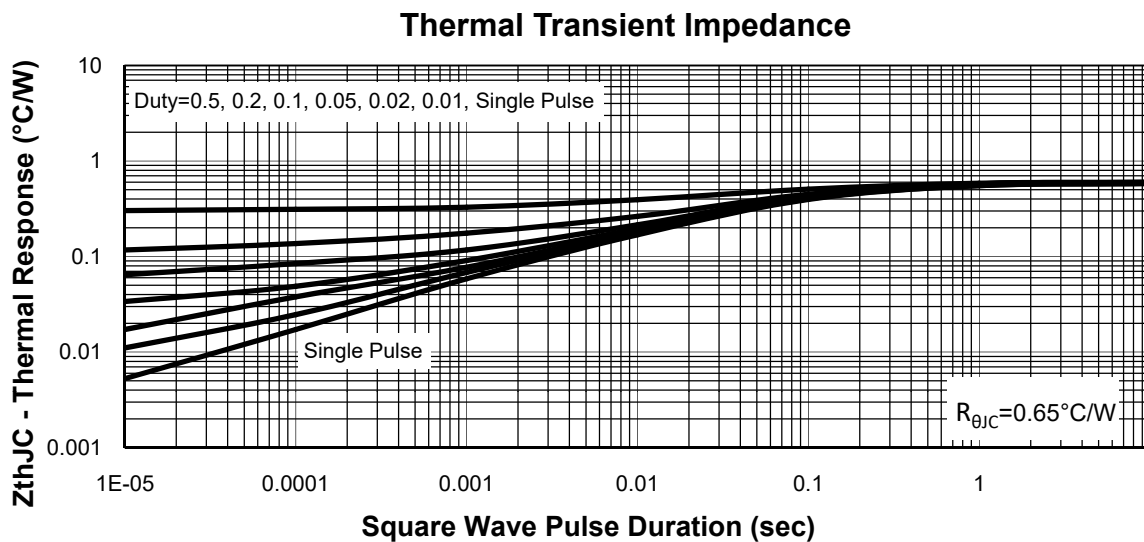
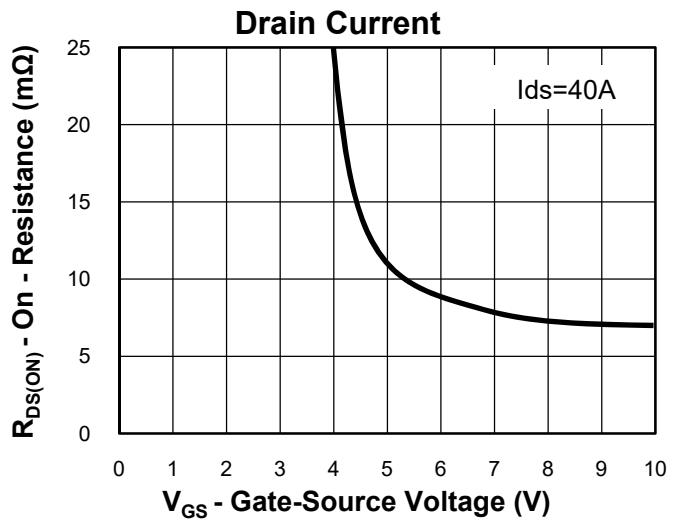
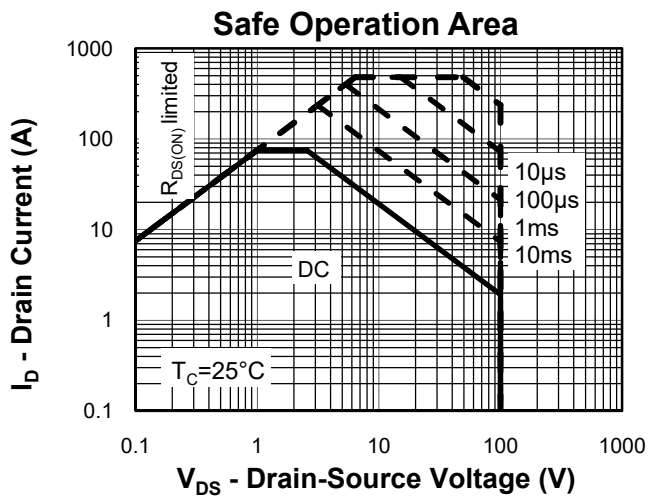
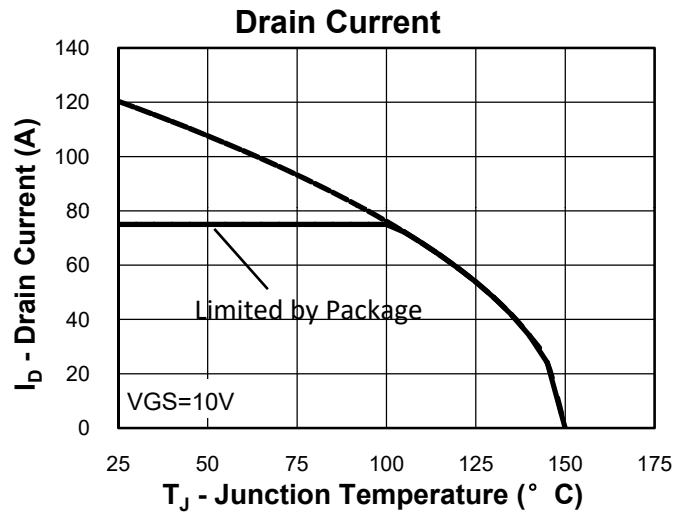
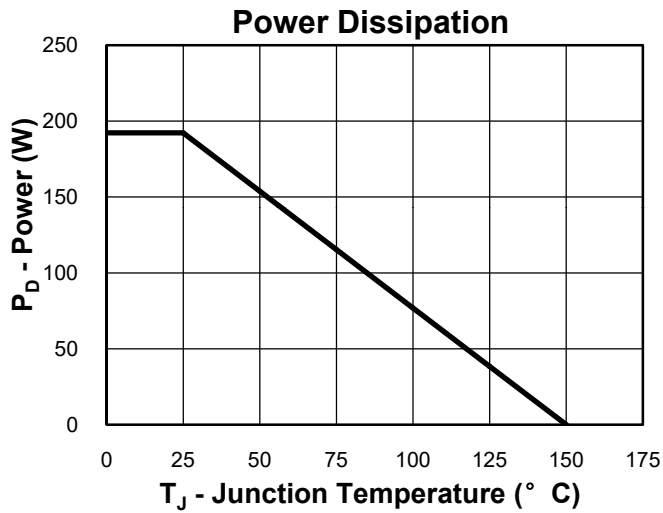
Ordering and Marking Information

Device	Package	Packaging	Quantity	Reel Size	Tape width
KS1202GA	TO-263	Tape&Reel	800	13"	24mm

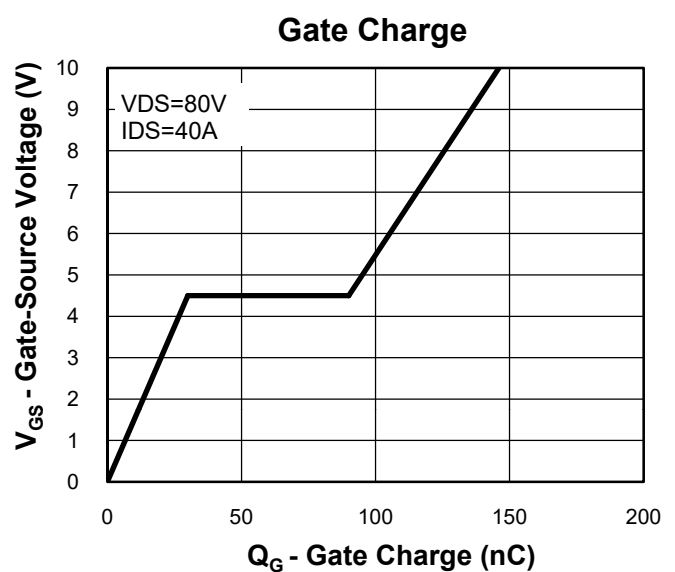
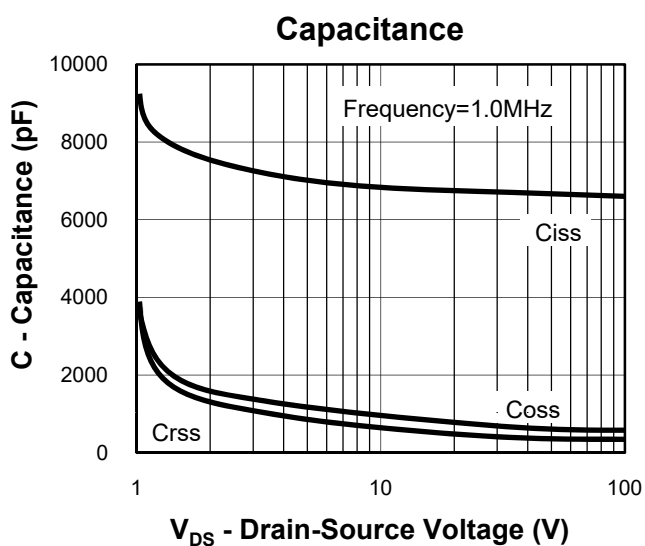
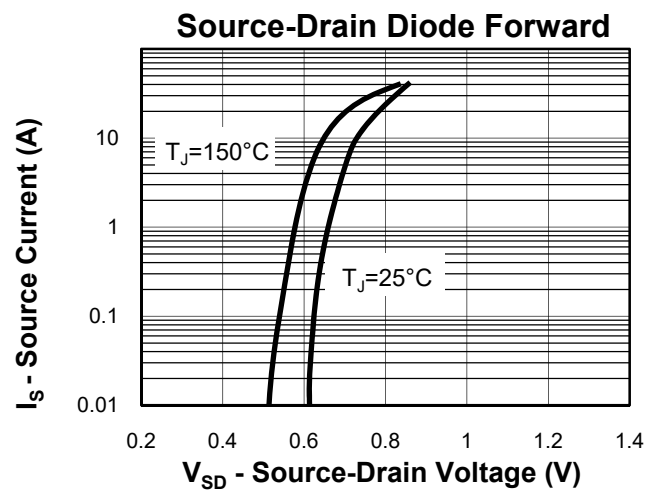
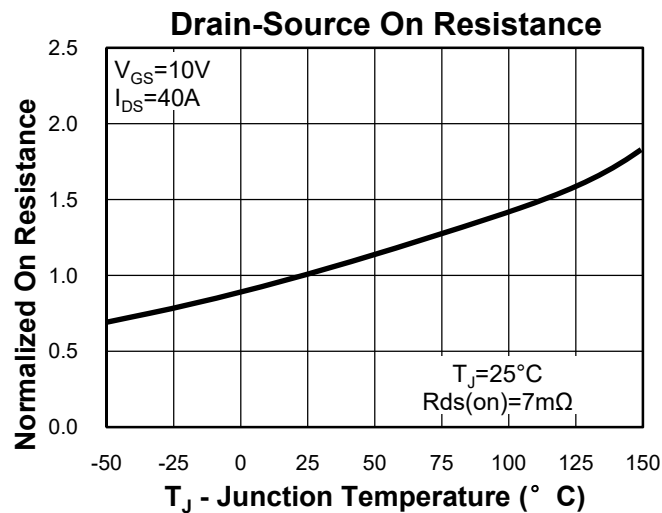
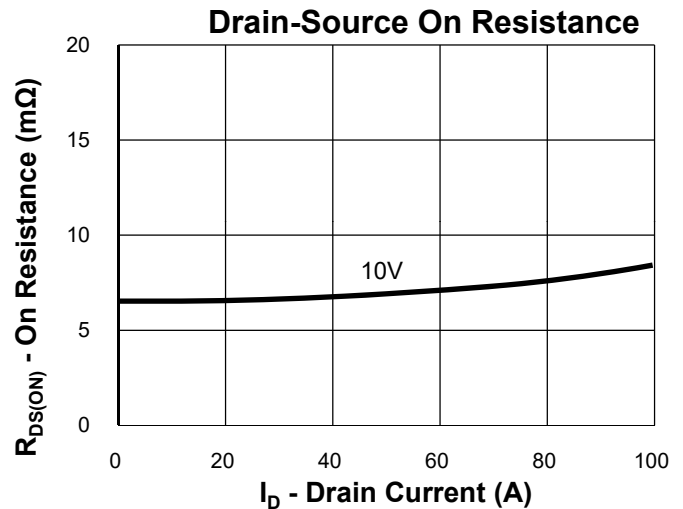
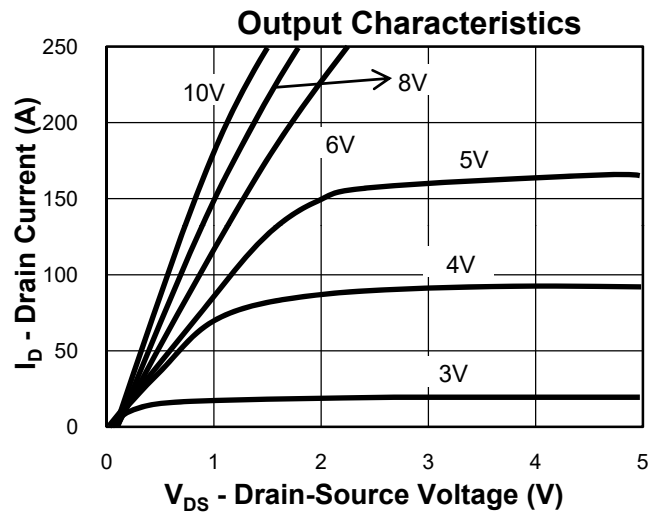


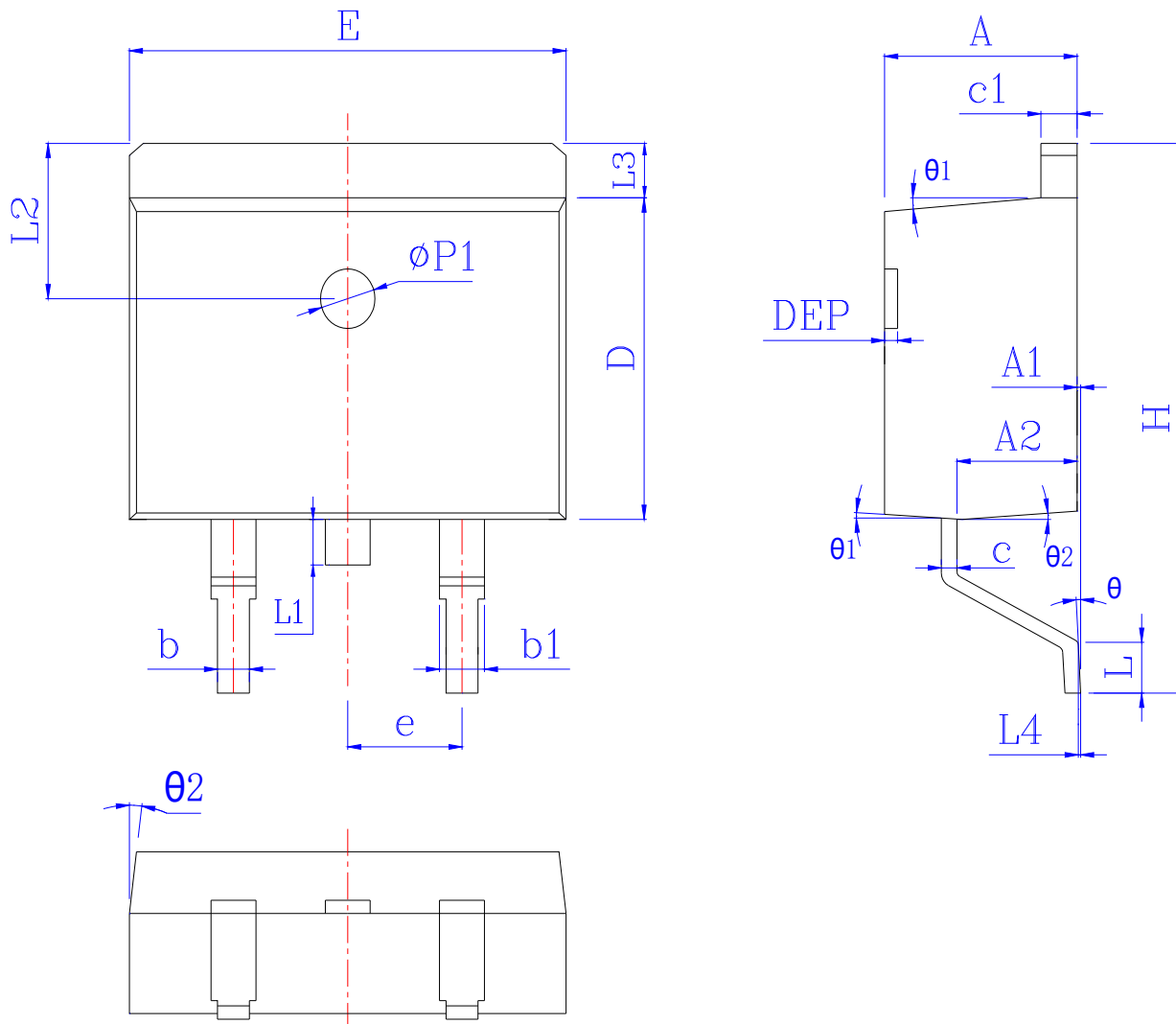
Y =Year,2017-A,2018-B,etc.
 WW =Week.
 XXX =Lot number.

Typical Characteristics



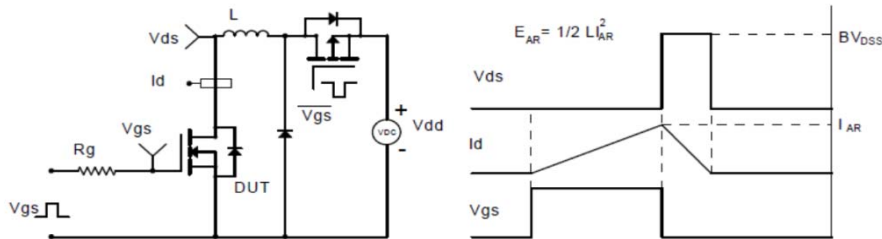
Typical Characteristics



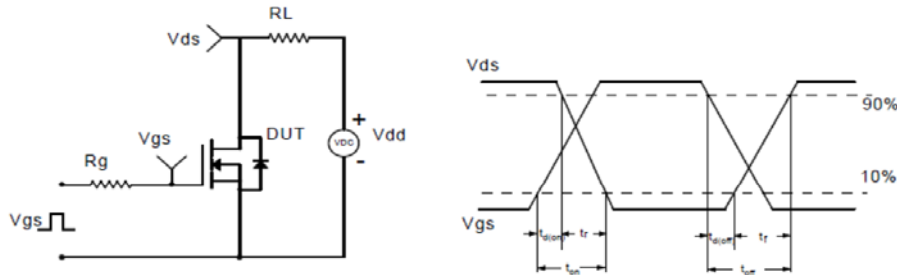
Package Information
TO-263


SYMBOL	MM			INCH			SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX		MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.55	4.72	0.173	0.179	0.186	L	1.94	2.30	2.60	0.076	0.091	0.102
A1	0.00	0.10	0.25	0.000	0.005	0.010	L3	1.17	1.29	1.40	0.046	0.051	0.055
A2	2.59	2.69	2.79	0.102	0.106	0.110	L1	*	*	1.70	*	*	0.067
b	0.76	*	0.90	0.030	*	0.035	L4	0.25 BSC			0.01 BSC		
b1	1.22	*	1.36	0.048	*	0.054	L2	2.50 REF			0.098 REF		
c	0.33	*	0.47	0.013	*	0.019	θ	0°	*	8°	0°	*	8°
c1	1.22	*	1.32	0.048	*	0.052	$\theta1$	5°	7°	9°	5°	7°	9°
D	8.60	*	9.29	0.339	*	0.366	$\theta2$	1°	3°	5°	1°	3°	5°
E	9.95	*	10.26	0.392	*	0.404	DEP	0.05	0.10	0.20	0.002	0.004	0.008
e	2.54BSC			0.100BSC			$\Phi p1$	1.40	1.50	1.60	0.055	0.059	0.063
H	14.70	15.10	15.79	0.579	0.594	0.622							

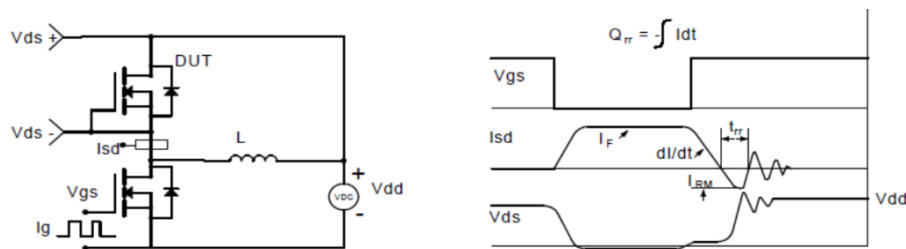
Avalanche Test Circuit and Waveforms



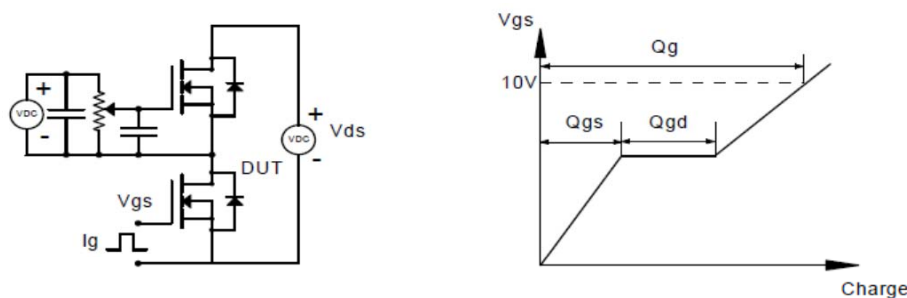
Switching Time Test Circuit and Waveforms



Diode Recovery Test Circuit and Waveforms



Gate Charge Test Circuit and Waveform



Customer Service

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