
# PH955L

## N-channel TrenchMOS logic level FET

Rev. 02 — 19 February 2009 Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

### 1.3 Applications

- DC-to-DC convertors
- General purpose power switching
- Motors, lamps and solenoids
- Portable equipment

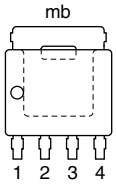
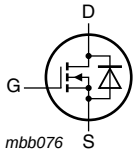
### 1.4 Quick reference data

**Table 1. Quick reference**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | - | 55 | V |
| $I_D$ | drain current | $T_{mb} = 25$ °C; $V_{GS} = 5$ V; see Figure 1; see Figure 3 | - | - | 62.5 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | - | - | 62.5 | W |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS} = 5$ V; $I_D = 25$ A; $V_{DS} = 44$ V; $T_j = 25$ °C; see Figure 11; see Figure 12 | - | 16.4 | - | nC |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 10 | - | 6.2 | 8.3 | mΩ |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |   SOT669 (LFPAK) |   |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PH955L | LFPAK | plastic single-ended surface-mounted package (LFPAK); 4 leads | SOT669 |

# 4. Limiting values

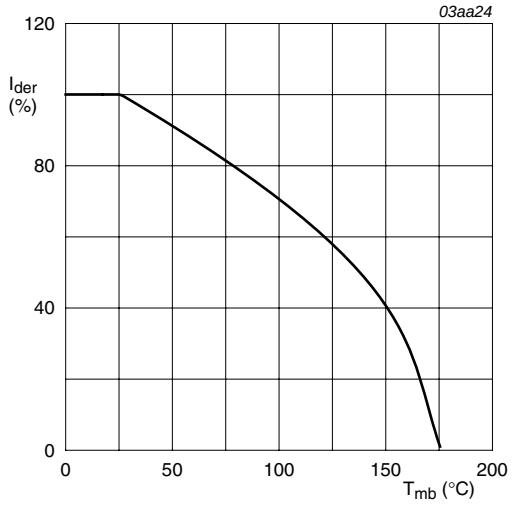
**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | | - | 55 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C; $R_{GS} = 20$ kΩ | | - | 55 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS} = 5$ V; $T_{mb} = 100$ °C; see Figure 1 | | - | 43.7 | A |
| | | $V_{GS} = 5$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3 | | - | 62.5 | A |
| $I_{DM}$ | peak drain current | $t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C; see Figure 3 | | - | 187 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; see Figure 2 | | - | 62.5 | W |
| $T_{stg}$ | storage temperature | | | -55 | 150 | °C |
| $T_j$ | junction temperature | | | -55 | 150 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb} = 25$ °C | | - | 52 | A |
| $I_{SM}$ | peak source current | $t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C | | - | 156 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)R}$ | repetitive drain-source avalanche energy | $V_{GS} = 5$ V; $I_D = 4.4$ A; $V_{sup} \leq 55$ V; unclamped; $t_p = 0.1$ ms; $R_{GS} = 50$ Ω | [1][2] | - | 2 | mJ |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; $I_D = 44$ A; $V_{sup} \leq 55$ V; unclamped; $t_p = 0.1$ ms; $R_{GS} = 50$ Ω | | - | 195 | mJ |

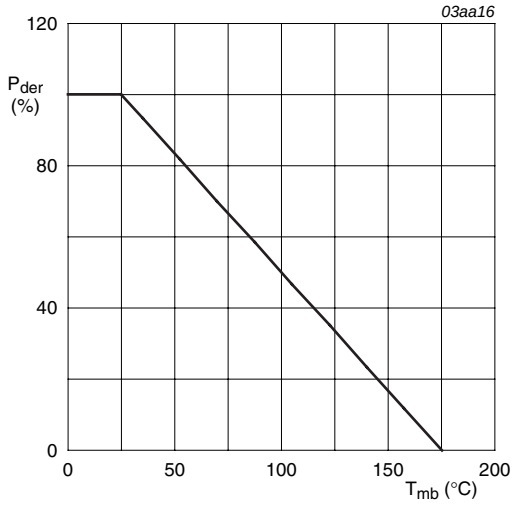
[1] Duty cycle is limited by the maximum junction temperature.

[2] Repetitive avalanche failure is not determined simply by thermal effects. Repetitive avalanche transients should only be applied for short bursts, not every switching cycle.



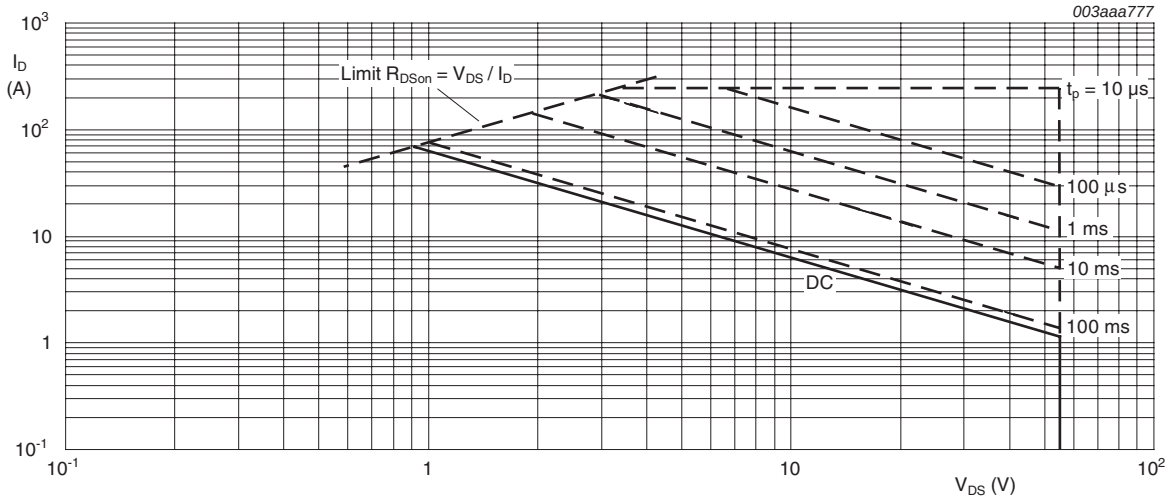

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**




$T_{mb} = 25°C; I_{DM}$ is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j\text{-}mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | - | 2 | K/W |

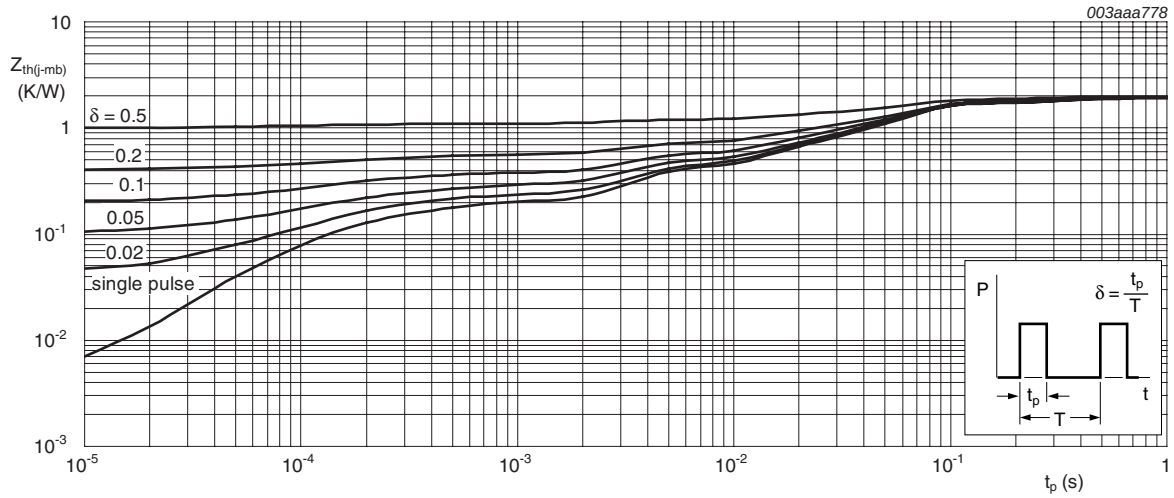
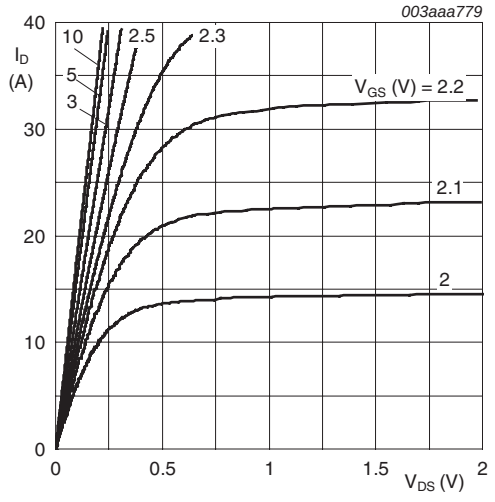



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 6. Characteristics

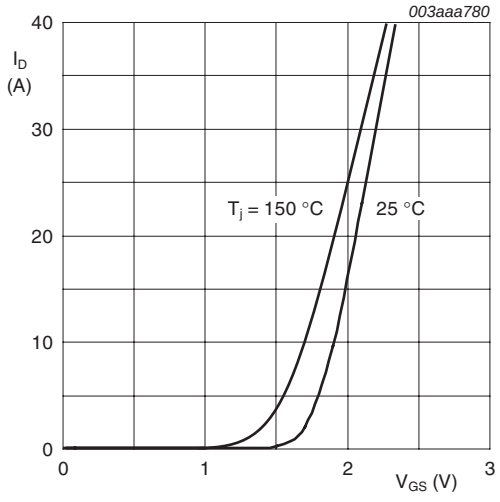
**Table 6. Characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | 50 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 55 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; see Figure 7; see Figure 8 | - | - | 2.3 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 150 °C; see Figure 7; see Figure 8 | 0.5 | - | - | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; see Figure 7; see Figure 8 | 1 | 1.5 | 2 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 55 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 55 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 15 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| | | $V_{GS}$ = -15 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 4.5 V; $I_D$ = 25 A; $T_j$ = 25 °C | - | 7.1 | 9.9 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 150 °C; see Figure 9 | - | - | 16 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see Figure 10 | - | 6.2 | 8.3 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 44 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; see Figure 11; see Figure 12 | - | 42 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 5.7 | - | nC |
| $Q_{GS1}$ | pre-threshold gate-source charge | | - | 4.3 | - | nC |
| $Q_{GS2}$ | post-threshold gate-source charge | | - | 1.4 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 16.4 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D$ = 25 A; $V_{DS}$ = 44 V; $T_j$ = 25 °C; see Figure 11; see Figure 12 | - | 2 | - | V |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 13 | - | 2836 | - | pF |
| $C_{oss}$ | output capacitance | | - | 441 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 210 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 25 V; $R_L$ = 1 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 4.7 Ω; $T_j$ = 25 °C | - | 18 | - | ns |
| $t_r$ | rise time | | - | 71 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 105 | - | ns |
| $t_f$ | fall time | | - | 25 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 14 | - | 0.85 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 30 V; $T_j$ = 25 °C | - | 62 | - | ns |
| $Q_r$ | recovered charge | | - | 48 | - | nC |



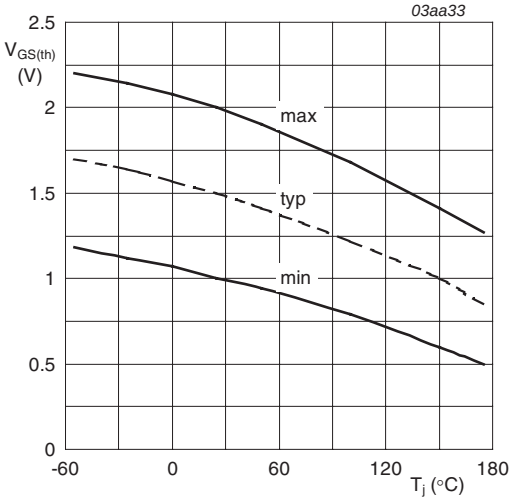

$T_j = 25°C$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



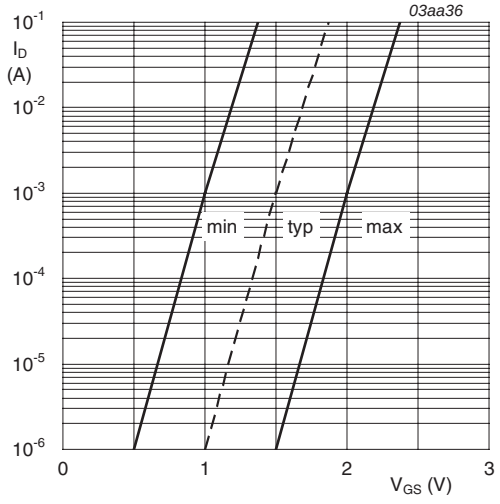

$T_j = 25°C \text{ and } 150°C; V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



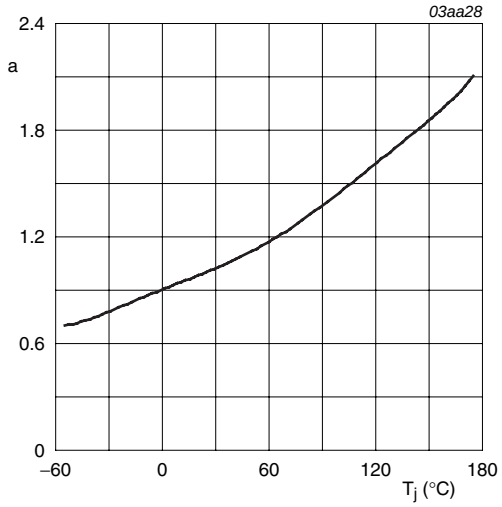

$I_D = 1mA; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



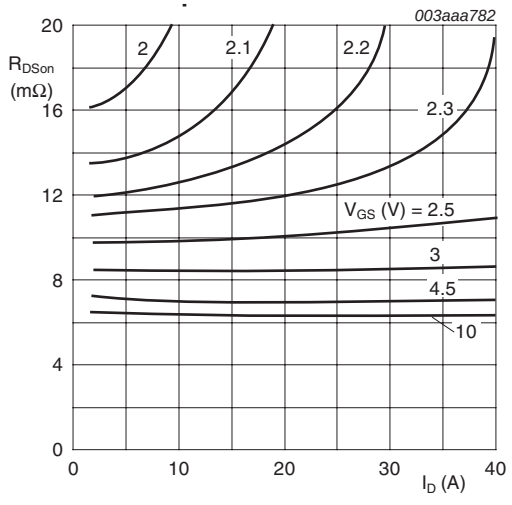

$T_j = 25°C; V_{DS} = V_{GS}$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



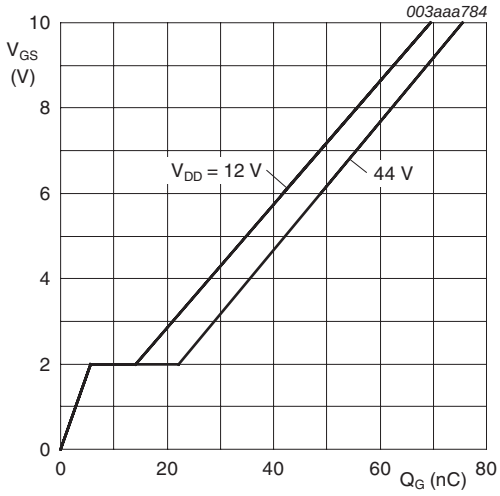

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature**




$$T_j = 25°C$$

**Fig 10. Drain-source on-state resistance as a function of drain current; typical values**




$$I_D = 25A; V_{DS} = 12V \text{ and } 44V$$

**Fig 11. Gate-source voltage as a function of gate charge; typical values**

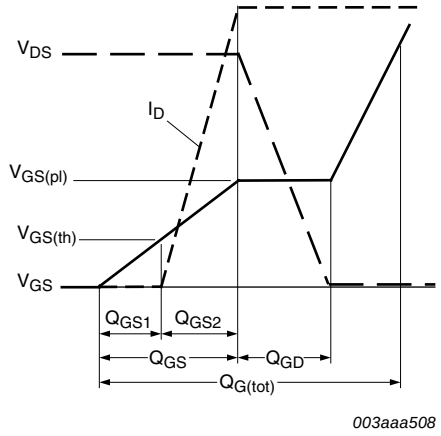
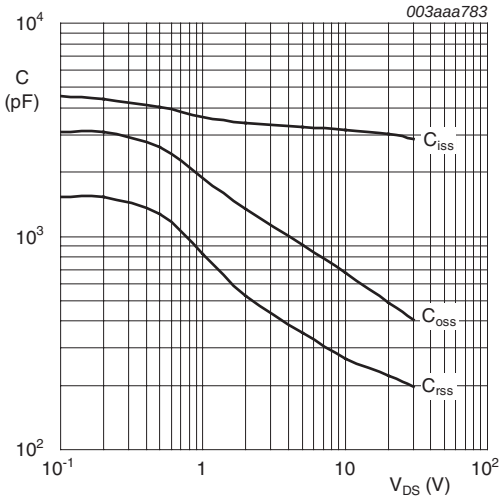
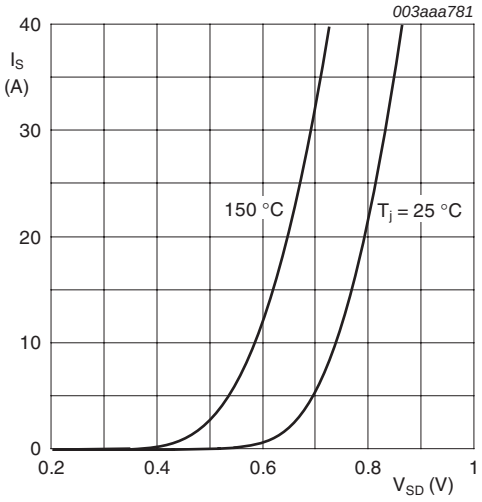



**Fig 12. Gate charge waveform definitions**




$V_{GS} = 0V; f = 1MHz$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

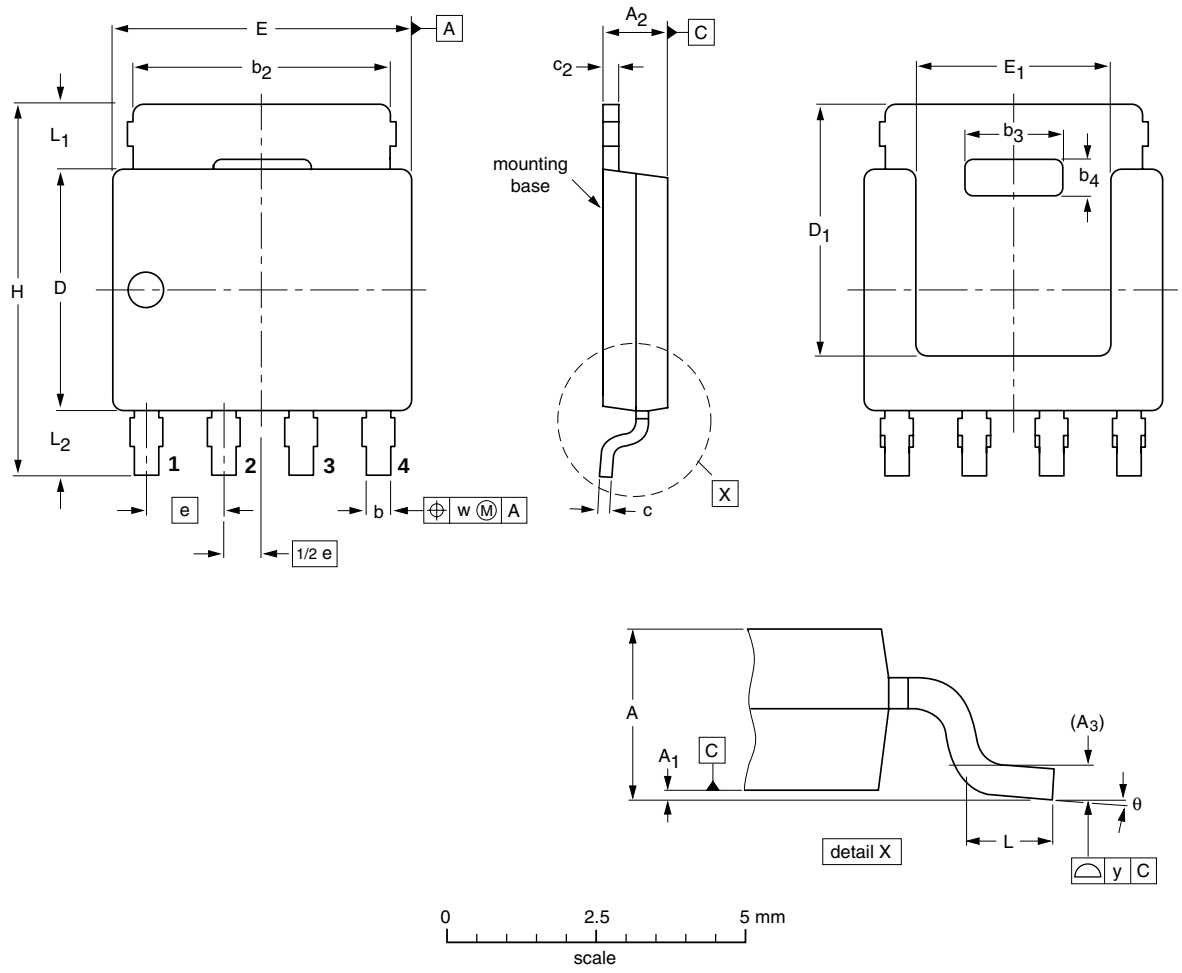



$T_j = 25°C \text{ and } 150°C; V_{GS} = 0V$

**Fig 14. Source current as a function of source-drain voltage; typical values**

# 7. Package outline

**Plastic single-ended surface-mounted package (LFPAK); 4 leads** **SOT669**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | $D^{(1)}$ | $D_1^{(1)}$ max | $E^{(1)}$ | $E_1^{(1)}$ | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.20<br>1.01 | 0.15<br>0.00 | 1.10<br>0.95 | 0.25 | 0.50<br>0.35 | 4.41<br>3.62 | 2.2<br>2.0 | 0.9<br>0.7 | 0.25<br>0.19 | 0.30<br>0.24 | 4.10<br>3.80 | 4.20 | 5.0<br>4.8 | 3.3<br>3.1 | 1.27 | 6.2<br>5.8 | 0.85<br>0.40 | 1.3<br>0.8 | 1.3<br>0.8 | 0.25 | 0.1 | 8°<br>0° |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~04-10-13~~<br>06-03-16 |

**Fig 15. Package outline SOT669 (LFPAK)**

# 8. Revision history

**Table 7. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PH955L_2 | 20090219 | Product data sheet | - | PH955L_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| PH955L_1<br>(9397 750 14557) | 20050301 | Product data sheet | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status [1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## 11. Contents





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